Review of Electronic Digital Computers

Joint AIEE-IRE Computer Conference

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REVIEW OF ELECTRONIC DIGITAL COMPUTERS

JOINT AIEE-IRE COMPUTER CONFERENCE

PAPERS AND DISCUSSIONS PRESENTED AT THE
JOINT AIEE-IRE COMPUTER CONFERENCE,
PHILADELPHIA, PA., DECEMBER 10–12, 1951

Sponsored by the

Committee on Computing Devices of the
American Institute of Electrical Engineers

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With the participation of the
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FOREWORD

The AIEE-IRE Computer Conference met on December 10–12, 1951, at Philadelphia to discuss the characteristics and performance of working, large-scale, electronic digital computers.

The conference was arranged by a joint committee appointed early in 1951 by the Committee on Computing Devices of the American Institute of Electrical Engineers and the Electronic Computers Committee of the Institute of Radio Engineers.

It was felt that the development of these machines had reached a point where useful engineering information could be drawn from the experience of the designers and users of these machines and that a published account of these machines, assembled in a report of this meeting, would be of permanent value in the development of engineering knowledge of this new field of activity.

The joint committee invited the co-operation of the Association for Computing Machinery, and representatives of that organization joined in the planning of the meeting and participated in the conference.

The extent of interest in the subject can be appreciated from the attendance at the conference, which totalled 877 members.

Descriptions of ten large-scale electronic computers of varying design and performance were presented, giving a cross-section of the varying designs to date of both parallel and serial types of electronic computers using storage devices including mercury delay lines, magnetic drums, and cathode-ray tubes. Other papers discussed detailed operating and component experience on certain of these calculators, and the final session summarized the present state of computer development and indicated some of the future possibilities of the Transistor in computer design.

At the luncheon meeting on the last day of the conference, an inspiring picture of the rapidly expanding use of large-scale computers in engineering design and analysis of our new airplanes, both commercial and military, gave the members of the conference a better understanding of the ultimate usefulness of their efforts.

During the conference, inspection trips gave many of the participants an opportunity to view the UNIVAC and the Burroughs Computer, and to visit the computer activities of the Moore School of Electrical Engineering of the University of Pennsylvania and of the Technitrol Engineering Company.

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Keynote Address

W. H. Mac WILLIAMS

MY purpose here at this conference is to provide a background, first for meetings like this on subjects dealing with computers, and second, for this particular meeting. My qualifications for keynoting are, I think, as good as those of anyone here: as far as this particular meeting is concerned, I am not now directly engaged in working on computers of the type that we are going to discuss; and the organization that I represent, the Bell Telephone Laboratories, is not in the business of making such computers. So I speak as a relatively innocent bystander.

This meeting, as your Chairman has indicated, is sponsored by the Joint AIEE-IRE Computer Committee, with assistance from the Association for Computing Machinery. It is a direct outgrowth of the successsful meeting a year ago at Atlantic City on electron tubes for computers. The Atlantic City meeting was initiated by Dr. A. L. Samuel as a representative of the Research Development Board, and was co-sponsored by the AIEE and IRE. Several factors were responsible for its success: it was timely; it permitted a thorough discussion of a small number of subjects; it brought together the divergent points of view of the manufacturer and the user; and it lasted long enough for the different points of view to be assimilated. These advantages can be obtained only rarely in the general meetings of the sponsoring societies because their large memberships include so many different interests.

These facts led Professor Brainerd to suggest the formation of the Joint AIEE-IRE Computer Committee, whose members are listed in the front matter of this book, to consider whether more meetings of the Atlantic City type should be held, and if so, on what subjects. We concluded that several subjects demanded attention, among them (1) a review of the useful results obtained from operating high-speed digital computers, (2) a comparison of the logic of these computers, (3) input and output equipment, (4) high-speed memory, and (5) choice of number system.

The first two subjects seemed to us to be the most urgent, and led us to arrange this meeting. We hope that you will tell us whether you too feel that such meetings are desirable, and that you will indicate in a positive way which subjects you consider most important. The start of this meeting is clearly too early to ask for your opinions, but after the meeting is over please let us have your views. We have arranged this meeting for *you*; let us know how you feel about it.

Now let's be more specific about *this* meeting.

A review of life in the field of large-scale digital computers will make it clear how timely this meeting is. Let me point out four phases of life in this field through which you have all passed, more or less together.

The phases were preceded by a period of pioneering, in which a relatively small number of people developed computers such as the ENIAC and the MARK I calculator.

The first phase I have called the future, or building, or talking phase. The common denominator was a remark somewhat like this: "What a wonderful critter our computer is going to be."

The second phase is what might be called the subjunctive, or debugging, or possibly the silent phase. The remarks that people made in this phase were, "It sure would be nice if we could get this thing to work."

The third phase is the present, or working, or bright-look phase, and the remarks that people made at this time were, "Our computer is working now, but we haven't had enough experience to judge it properly."

The fourth I have called the past or getting-results phase. This again is a talking phase, and people tend to say nowadays, "It has been working fine; we are glad we built it, but we wish we had done this and this instead of what we actually did. However, we are going to fix that in our new model, and besides we are going to make it a lot simpler and more reliable."

It is because of this latter phase that we have scheduled this meeting now. Computer people have had enough experience to judge the large machines that they have produced, and it is appropriate to take stock now, before people get too far along on the new round of machines which is being started.

We may now state formally the purpose of this meeting: namely, to assess the adequacy of the designs of present working high-speed digital computers in order to point out the direction in which computer design should go, to make computers best for the jobs that they have been doing and for the jobs that they will have to do.

This is basically an engineering or design objective, but it is clear that it also involves the users in an important way. This is a meeting of both builders and users, all of whom are actively interested in the field. It is a topical meeting because many people are looking around and deciding how to make new machines, for both civil and military purposes.

A sensible assessment of the computers requires a study of their comparative anatomy; that is, a comparison of the logics of their design. Summaries of logic have been included in the indiviual papers.

Published material in this field has been rather sparse. Only a few machines have been well written up in material available to the general public. An important objective of this meeting has been to provide published proceedings that will be available to everyone. Much of the material on detailed subjects such as logic will be presented in abbreviated form, but the written material for the proceedings has not been cut. We have aimed to make the published proceedings a record of the characteristics and usefulness of new operating high-speed computers.

Most of the papers in this meeting are devoted to computers which are now in use. It has been our aim to combine the points of view of the builder and the user. In the case of the UNIVAC, we have papers by both the designer and the user, since they are separate groups. There have been two cases where we have not been able to follow this practice. In the case of the Harvard MARK III calculator, we have information from the user only, since the designer has already spoken at length about this machine. And in the case of the ERA-1101, we have information from the builder only, because the user is not free to talk about his classified applications.

There are three papers on the program that do not relate directly to individual machines.

First, there is a report by one of the most prominent users of computing equipment, which will deal with en-

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gineering applications of computers. This report will be given by Mr. C. R. Strang of the Douglas Aircraft Company.

There also is on the program a paper on the application of transistors to digital computation, since these devices have tremendous possibilities for cutting down power consumption, computer size . . . . I had better stop myself before I give you a sales talk. The paper will be presented by Mr. J. H. Felker.

An important objective of this meeting is to indicate desirable design trends. To assist in this objective and to start general discussion, the last paper will be a summary of the material presented and a forecast of the future of computers, by Mr. J. W. Forrester.

One could say really that we have been optimists to schedule a meeting like this. We feel that in addition to keeping computer engineers employed—in itself a praiseworthy objective—a great deal of worthwhile experience has been obtained from the perhaps $30,000,000 that have been spent so far on large high-speed digital computers. It is important to get the most out of the experience resulting from this large amount of work, so that our new machines can be made as good as possible.

We hope that this meeting will enable you to do just that. Please let us know how you like the meeting and what suggestions you have for other similar meetings.

The UNIVAC System

J. PRESPER ECKERT, JR.
JAMES R. WEINER
H. FRAZER WELSH
HERBERT F. MITCHELL

Organization of the UNIVAC System

IN March 1951, the first UNIVAC* system formally passed its acceptance tests and was put promptly into operation by the Bureau of the Census. Since the UNIVAC is the first computer which can handle both alphabetic and numerical data to reach full-scale operation so far, its operating record and a review of the types of problems to which it has been applied provide an interesting milestone in the ever-widening field of electronic digital computers.

The organization of the UNIVAC is such that those functions which do not directly require the main computer are performed by separate auxiliary units each having its own power supply. Thus the keyboard to magnetic tape, punched card to magnetic tape and tape to typewritten copy operations are delegated to auxiliary components.

The main computer assembly includes all of those units which are directly concerned with the main or central computer operations. A block diagram of this arrangement is shown in Figure 1. All of the elements shown are contained within the central computer casework except the supervisory control desk (*SC*) and the Uniservos,* to which the lines in the upper right section of the diagram connect.

The supervisory control, in addition to all the necessary control switches and indicator lights, contains an input keyboard. Also cabled to the supervisory control is a typewriter which is operable by the main computer. By means of these two units, limited amounts of information can be inserted or removed either at the will of the operator or by the programmed instructions.

The input-output circuits operate on all data entering or leaving the computer. The input and output synchronizers properly time the incoming or outgoing data for either the Uniservos (tape devices) or the supervisory control devices. The input and output registers (*I* and *O*) are each 60 word (720 characters) temporary storage registers which are intermediate between the main computer and the input-output devices.

The high-speed bus amplifier is a switching central through which all data must pass during transfer between any arithmetic register and the main memory or between the memory and the input-output registers. The arithmetic registers are shown along the bottom of diagram each connected to the high speed bus system.

The *L*-, *F*-, *X*-, and *A*-registers are each of one word or 12-character capacity and are directly concerned with the arithmetic operations. The *V*- and *Y*- registers are of 2- and 10-word capacity, respectively. They are used solely for multiple word transfers within the main memory. Associated with the arithmetic registers are the algebraic adder (*AA*), the comparator (*CP*), and the multiplier quotient counter (*MQC*).

Addition-Subtraction Instructions

The addition-subtraction operations are performed in conjunction with the comparator since all numerical quantities are absolute magnitudes with an algebraic sign attached. Before either an addition or subtraction is performed, the two quantities, one already in the *A*-register and the other either from the memory or from the *X*-register, depending upon the particular instruction, are compared for magnitude and sign. The adder inputs can then be switched so as always to produce a noncomplemented result for any operation. The choice of adder input arrangement is therefore under the control of the comparator. The comparator also determines the proper sign for the result according to the usual algebraic rules.

One additional function performed by the comparator for addition and subtraction is to control the complementer. This determination is based upon which operation (+, or −) is indicated, and, whether the signs are like or unlike. For a subtract instruction, the sign of the subtrahend is reversed before entering the comparator. The comparator then compares the signs of the quantities in order to

* Registered trade mark.

J. Presper Eckert, Jr., James R. Weiner, H. Frazer Welsh, and Herbert F. Mitchell are all with Eckert-Mauchly Computer Corporation, Division of Remington Rand, Philadelphia, Pa.

The UNIVAC System has been an over-all company project and hundreds of people have participated. It is, therefore, difficult to acknowledge the contributions of individuals. However, special mention must be made of the contributions of Mr. H. Lukoff, Mr. E. I. Blumenthal, Mr. L. D. Wilson, and Mr. J. D. Chapline, Jr. To the Census Bureau a great debt of gratitude is owed for their continuous support of this project.

determine whether the two quantities are subtracted or added.

Multiplication Instruction

The multiplication process requires the services of the adder, the comparator, the multiplier-quotient counter and the four arithmetic registers. During the first step of multiplication the X-register receives the multiplier from the memory and the comparator determines the sign of the final product by comparing the signs of the multiplier and multiplicand. During the next three steps the multiplicand, which has been stored in the L-register by some previous instruction, is transferred three times to the A-register through the algebraic adder. The result, three times the multiplicand, is then stored in the F-register. During the next 11 steps of multiplication, the successive multiplier digits, beginning with the least significant, are transferred from the X-register to the multiplier-quotient counter. The multiplier-quotient counter then determines whether each particular multiplier digit is less than three, or greater than or equal to three.

If the former, the L-register releases the multiplicand to the A-register via the adder, and the multiplier-quotient counter is stepped downward one unit. If the multiplier digit is equal to or greater than three, the multiplier-quotient counter sends a signal to the F-register which releases three times the multiplicand to the A-register and the multiplier-quotient counter is stepped three times. Thus a multiplier digit of seven would be processed as two transfers from the F-register to the A-register and one transfer from the L-register to the A-register, or a total of three transfers.

When the multiplier-quotient counter reaches zero, the next multiplier digit is brought in from the X-register, while the A-register, containing the first partial product, is shifted one position to the right.

During the final step of multiplication, the sign is attached to the product which has been built up in the A-register. One of the several available multiplication instructions causes the least significant digits, as they are shifted beyond the limits of the A-register, to be transferred to the X-register where they replace the multiplier digits as they are moved to the multiplier-quotient counter. Thus 22 place products can be obtained as well as 11 place.

Division Instruction

The division operation is performed by a nonrestoring method. The divisor is stored in the L-register by some previous instruction and the dividend is brought from the memory and put in the A-register during the first step of the division instruction. As in multiplication, the signs of the two operands are compared in the comparator at this time and the sign of the quotient is then stored in the comparator pending completion of the division operation. The principal stages of division consist of transferring the divisor from the L-register to the A-register through the complementer and adder as many times as required to produce a quantity less than zero in the A-register, the dividend having been first shifted one position to the left. The multiplier-quotient counter counts each transfer, thereby building up the first quotient digit. As soon as the quantity in the A-register, (neglecting its original sign) goes negative, the digit in the multiplier-quotient counter, not counting the transfer which causes the remainder to go negative, is transferred to the X-register and the remainder in the A-register is shifted one place to the left. The divisor is then added to the A-register until the quantity becomes positive. This time the multiplier-quotient counter must give the complement of the number of transfers for the real quotient digit. Special complementing read-out gates provide this method of interpreting the multiplier-quotient counter.

The X-register therefore collects the quotient, digit by digit, from the multiplier-quotient counter until the full 11 digits have been obtained. The quotient is then transferred to the A-register and the sign from the comparator (CP) is affixed during the final stage of the divide instruction.

The other internal operations of the UNIVAC include many transfer instructions by which words may be moved among the registers and memory with and without clearing, the extraction instruction by which certain digits of a word may be extracted into another word according to the parity of the corresponding digits of an extractor word; shift instructions; and special control instructions such as breakpoint, transfer of control, (explained in subsequent paragraphs) and stop.

Basic Operating Cycle

The basic operating cycle of the UNIVAC is founded upon single address instructions which specify the memory location of one word. In the case of the arithmetic instructions which require two operands, one of the operands must be moved into the proper register by some previous instruction. In order to control the sequence of instructions, a special counter, called the control counter (CC), retains the memory location from which the succeeding instruction word is to be obtained. Each time a new instruction word is received from the memory, the quantity in the control counter is passed through the adder where a unit is added to it. Therefore the normal sequence is to refer to successive memory locations for successive instruction words. Initially the control counter is cleared to zero and the first group of instructions must, therefore, be placed in memory locations from zero upward. A transfer of control instruction enables the programmer to change the control counter reading whenever desired and thus shift from one sequence to another. After a transfer of control takes place, the new number in the control counter is increased by unity each time a new instruction word is obtained from the memory.

Transfer of Control Instructions

The transfer of control instructions are of three types, the unconditional transfer which changes the control counter reading without question, and two conditional instructions which require that either equality or a specific inequality exists between the words in the A-register and the L-register. In the former case the quantities must be identical for transfer of control to occur and in the latter the quantity in the A-register must be greater than the quantity in the L-register for the control counter reading to be changed.

Since the UNIVAC can handle alphabetic as well as numerical data, these conditional transfer instructions are as useful for alphabetizing as they are to determine if a certain iterative arithmetic process has been performed often enough to come within specified numerical tolerances.

Control Register

Since six characters (intermixed alphabetic and numerical) are sufficient to specify an instruction and there are 12 characters per word, each instruction word can represent two independent instructions. A 1-word register, called the control register (CR), has been provided, which stores each instruction word as it comes from the memory. Thus one memory referral is sufficient for a pair of instructions and the control register stores both halves so that the second instruction is available as soon as the first has been completed.

The general term control circuits includes all those elements which work together to process the instruction rou-

tine. As each instruction word reaches the control register, the first half of it is passed immediately into the static register (*SR*). The static register drives the main function table and memory switch. The instruction digits are translated by the function table into the appropriate control signals for the instruction called for. The memory switch selects the location called for by the memory location digits and opens the proper memory channel to the high-speed bus system at the proper time. Since the memory is constructed of 100 channels, each holding ten words, the memory switch is a combination of spatial and temporal selection.

Cycle Counter

Implicit within each instruction, as translated by the function table, is an ending signal which causes the computer to move on to the next instruction. The key to this sequence is the cycle counter (*CY*), which is advanced by the ending pulse. The cycle counter is a 2-stage 4-position counter, which is connected into the function table. By virtue of this relation, *CY* develops signals in addition to those developed by the instruction, which, for example, can cause the control register to transfer the second half of the instruction word into the static register when the first half has been completed. Similarly, after the second half instruction is finished the cycle counter causes the reading of the control counter to pass into the memory location section of the static register and thus cause the next instruction word to be transferred from the memory to the control register. When the word reaches the control register, the cycle counter also causes the control counter reading to be increased by unity. The four cycles are designated by the first four Greek letters α (transfer *CC* to *SR*), β (transfer memory to *CR*), γ (perform first instruction), and δ (perform second instruction).

Program Counter

The multistage instructions, such as multiplication, are guided through their various steps by the program counter (*PC*). The program counter has four stages or 16 positions. All multistage instructions can be performed within this number of steps.

Checking Circuits

The checking circuits of the UNIVAC are of two main types, odd even checkers and duplicated equipment with comparison circuits. The odd-even checker depends upon the design of the pulse code used within the computer. This code provides seven pulse positions for every character. Six of the seven positions are significant as the actual code while the seventh is the odd-even channel. If the number of pulses or ones within the first six channels of any character is even, a one is placed in the seventh channel to make the total odd. Thus, the total number of ones across the seven channels is always odd. By means of a binary counter and a few gates, an odd-even checker has been constructed which examines every seven pulse group which passes through the high speed bus amplifier. In this connection, mention must be made of the periodic memory check which interrupts operation every five seconds to pass the entire contents of the memory over the high speed bus system and, consequently, through the odd-even checker. Any discrepancy is immediately signalled to the supervisory control and further operation ceases.

The duplicated equipment type of checking consists of duplicating the most essential parts of the arithmetic circuits and their controls and producing simultaneously independent results, which can then be compared for equality. For this type of checking, the *A*-, *F*-, *X*-, and *L*-registers, algebraic adder, comparator, multiplier-quotient counter, and the high speed bus amplifier are duplicated.

The memory is not duplicated, but is checked by the periodic memory check mentioned previously. Various sections of the control circuits are duplicated such as the program counter and cycle counter.

Timing Pulse Generator and Cycling Unit

The timing pulse generator and cycling unit (*CU*) are the source of the basic timing signals throughout the computer. The timing pulses occur at 2.25 megacycles per second. The cycling unit subdivides this rate into the character rate and word rate. The character rate is one seventh of the basic pulse rate since there are seven pulses for each character. There are 12 characters per word but space for a 13th character is included in a word time and is called the space between words. This time is used for switching purposes.

The cycling unit, therefore, develops the word signals at $1/7 \times 1/13$ or $1/91$ of the basic pulse rate. Within the cycling unit (*CU*) are numerous duplications and comparisons to ensure complete reliability.

Input Output Circuits

The operation of the input-output system is dovetailed as efficiently as possible with the operation of the arithmetic circuits. Whenever possible, parallel operations are allowed to proceed so as to minimize the time lost on internal operation while the slower input-output operations are taking place.

The principal input-output instructions are handled in a manner identical to that for the internal operations, except that now the function table develops signals which bring the input-output control circuits into operation. The information supplied to the input-output control circuits by the function table includes the following:

1. Which of the ten possible Uniservos is being called on.
2. Whether it is a read or write, that is, an input or output operation.
3. If it is "read," the direction in which the tape is to move.

The input-output control circuits, therefore, begin by testing whether or not the Uniservo indicated now is in use or not. If it is already in use, everything else waits until that Uniservo is free. Next, the input-output control circuits test to determine whether the Uniservo selected last moved backward or forward. If the previous direction does not agree with the new direction called for, the input-output control circuits generate the proper signals to prepare the Uniservo to move in the opposite direction. If the instruction is to rewind a Uniservo, the input-output control circuits then direct the center drive of the selected Uniservo to rewind the tape to the beginning and stop.

As soon as the instruction has proceeded to the point where the input-output control circuits need no further information from the function table, the instruction ending signal is generated and the internal circuits proceed to the next instruction, even while the reading, writing or rewinding continues. The UNIVAC can process an input, an output and several rewind operations while simultaneously carrying on internal computation.

So far the method by which the words are transferred from the *I*-register to the memory has not been mentioned. This operation is combined with certain read instructions in a manner not immediately obvious. There are two instructions which read from the tape to the *I*-register, one causing the tape to move forward, the other causing it to move backward There are two other

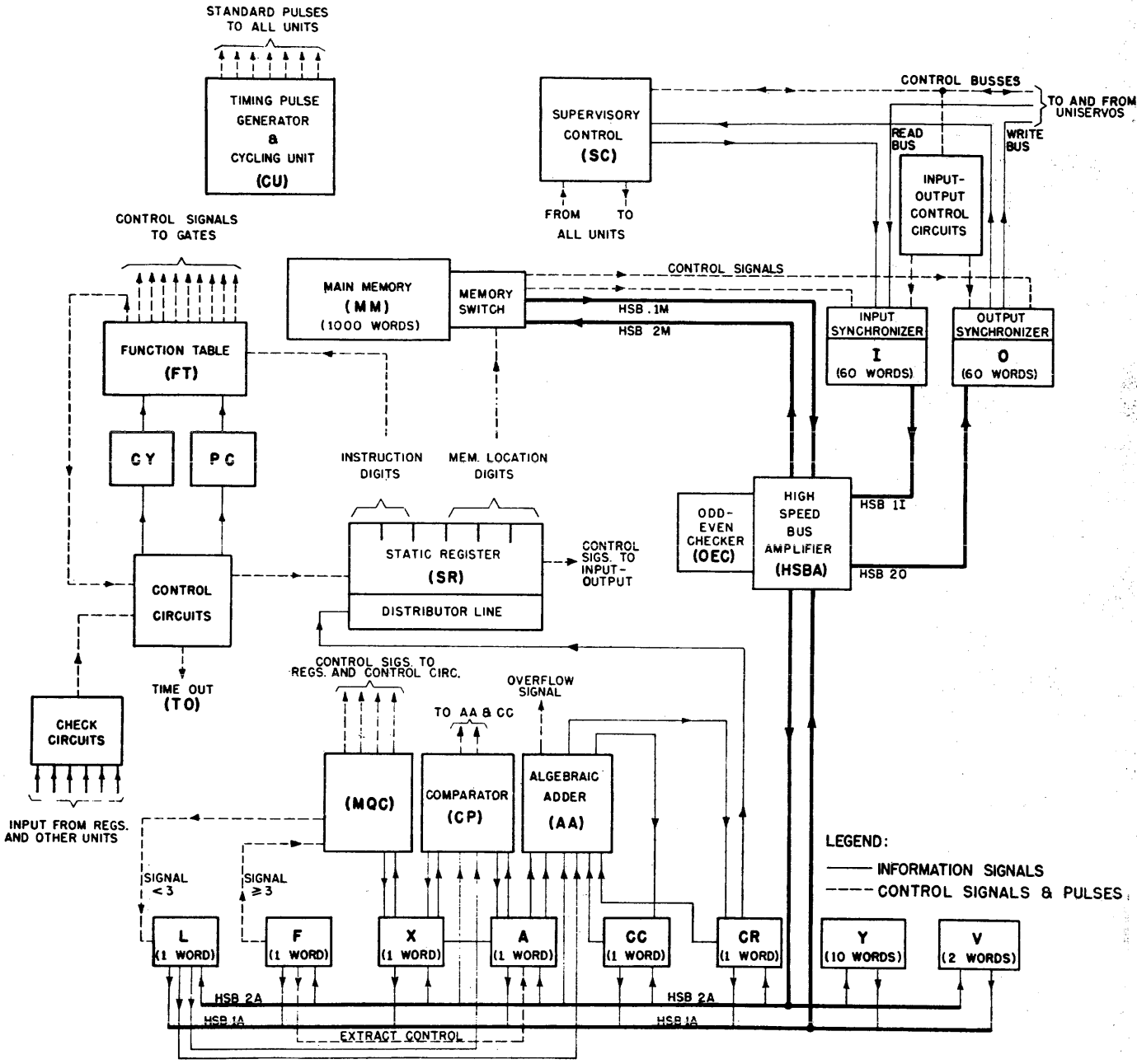

Figure 1. Block diagram of UNIVAC

input instructions similar to those just mentioned, but they have the additional operation of first reading from the *I*-register to the memory and then reading a new group of 60 words from tape into the *I*-register. Thus the first type of input instruction reads from tape to the *I*-register only. It must be followed by the second type of instruction in order first to clear the *I*-register and then read in the second block of 60 words.

The output instructions do not operate in this way but instead read directly from memory to the *O*-register and then to the tape as one instruction.

A third type of checking circuit occurs in the input-output control circuits which counts the number of characters transferred from the tape in each block. Since there must always be 720 characters per block, the 720 checker signals any discrepancy to the supervisory control.

One other phase of the input-output operation concerns the two supervisory control input-output instructions. One of them permits a single word to be typed in from the input keyboard and the other causes a single word to be typed out automatically.

Auxiliary Equipment

The two principal auxiliary devices mentioned earlier were the Unityper,* which converts keyboard operations to tape recording, and the Uniprinter,* which converts magnetic recording to typewritten copy.

Unityper

A simple block diagram of the Unityper is shown in Figure 2. Each keyboard operation pulses the input to an encoding function table which, in turn, drives the appropriate heads for recording the particular combination on the tape. Simultaneously, the same pulse triggers a motor delay flop which operates the tape motor for an interval sufficient to move the tape across the head for the distance required to record one character. However, there is a punched paper loop system associated

* Registered trade mark.

with the Unityper for the purpose of providing the typist with various guideposts individually set up for each problem. The loop control system serves three distinct control functions. First, it allows the programmer to set up various numbers of characters for the individual items being entered for a given problem. If the typist ever enters other than the specified number of characters, the loop control signals an error. Although the basic word length is 12 characters, the programmer may subdivide or group the words to suit any length of item. The loop can then be punched with what are called "force check" punches. Whenever the typist completes a correctly entered item, she must operate a release key before entering the next item. If the forced check is released too early an error is created, or if an additional character is typed after the forced check should have been released, an error is similarly indicated.

The second function of the loop is to control the erase operation. The erase operation is the only way in which an error can be recalled. When the erase key is operated, the loop and tape are both stepped backward until a stop punch (usually associated with each forced check) is encountered. Thus the entire erroneous item is erased, and at a much higher rate than that at which the backspace key can be operated. The backspace, incidentally, cannot cancel an error indication, but it can be used to correct a wrongly typed character if the typist recognizes it.

The third function of the loop system is to enter, automatically, various fill-in characters. Under one such system of operation, the loop control records the characters only at the behest of the operator. This function is useful where individual entries, such as personal names, do not fill out all of the space allotted. The other operation is fully automatic in which the loop assumes full control to record, for example, a group of fill-in characters later to be replaced by computed data within the central computer.

The block diagram therefore shows the loop motor connected to the same delay flop that steps the tape motor. The same signal which moves the two motors also sets a second delay flop, (*DF2*) which produces a delayed probing pulse. The probing pulse examines the paper loop photoelectrically for the new combination. A third delay flop (*DF3*) produces another probing pulse after the relays associated with the loop photocells have had time to set up. If any automatic function is indicated by the photocells, the probing pulse passes through the interpreting relays, enters the encoding function table to generate the fill-in characters, and thus starts the cycle over again. All automatic functions take place at about 22 characters per second.

Numerous odd-even checks are introduced in the Unityper to provide checks on tape and loop motion and on the recorded code combination.

Uniprinter

The Uniprinter is shown in simplified block diagram in Figure 3. Its operation is a simple cycle which is initiated by a start button. The start button triggers the motor flip-flop (*MFF*). The motor pulls the tape across the reading head until a combination is detected. The presence of pulses on any of the seven lines between the reading head and the relay decoding function table is sufficient to restore the motor flip-flop (*MFF*) and stop the tape motion. Simultaneously a print delay flop (*DF1*) is triggered. During the delay flop interval, the decoding relays are given time to set up. When the delay flop recovers, a pulse is sent through the relay table which reappears at one of the typewriter magnetic actuators. As the typebar reaches the platen, a printer action switch (*PAS*) is operated which pulses the motor flip-flop and starts a new search for the next character on the tape. The odd-even properties of the UNIVAC pulse code are utilized for checking purposes.

ENGINEERING ASPECTS

The entire UNIVAC system is constructed of circuits which are as conservative as is consistent with the desired reliability and speeds of operation. The circuits have been designed as building blocks and the entire computer is constructed around these blocks.

One of the most important of these blocks is the pulse reshaping circuit which consists of a timing pulse gate and a fast acting flip-flop which generates the pulse envelope equivalent of the gated timing pulses. Two polarities of timing pulse are used, the one being capable of tripping the flip-flop into one state, the other polarity of tripping it to the other state. As a deteriorated pulse envelope is applied to the timing pulse gate input, either one or the other polarity of pulse is always gated. The flip-flop therefore produces a sharpened and correctly timed output waveform.

The gating and switching circuits in the central computer are constructed of germanium crystal diodes, which include the main and subordinate function tables.

The registers are all circulating delay type using a mercury tank of one, two, or ten word-times of delay, except the static register. The latter is composed of 27 flip-flops which are required to maintain the static signals applied to the function tables, for at least an entire word-time.

The switching time allowed by the seven pulse-times of the space between words is, in general, not sufficient for a new function table excitation to stabilize. Therefore the time-out system, used successfully in the BINAC, also is employed in the UNIVAC. Whenever an ending pulse is generated, or any other pulse which indicates that a new set of control signals are required from the function table, an interval of one

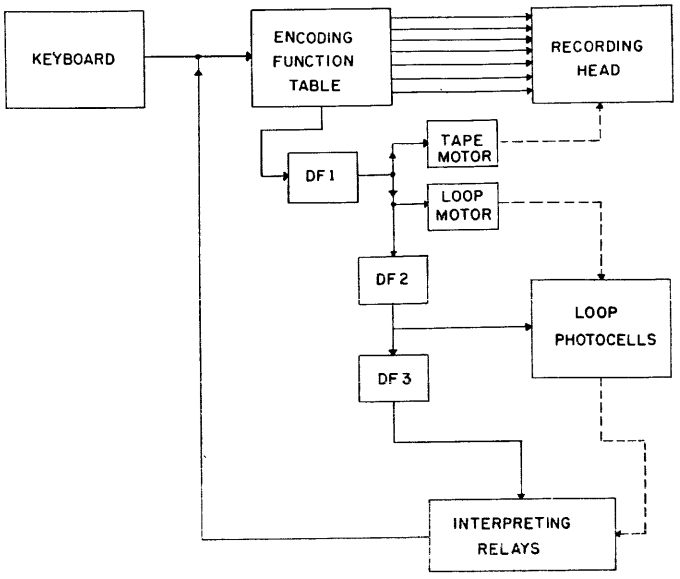

Figure 2. Simplified block diagram of Unityper

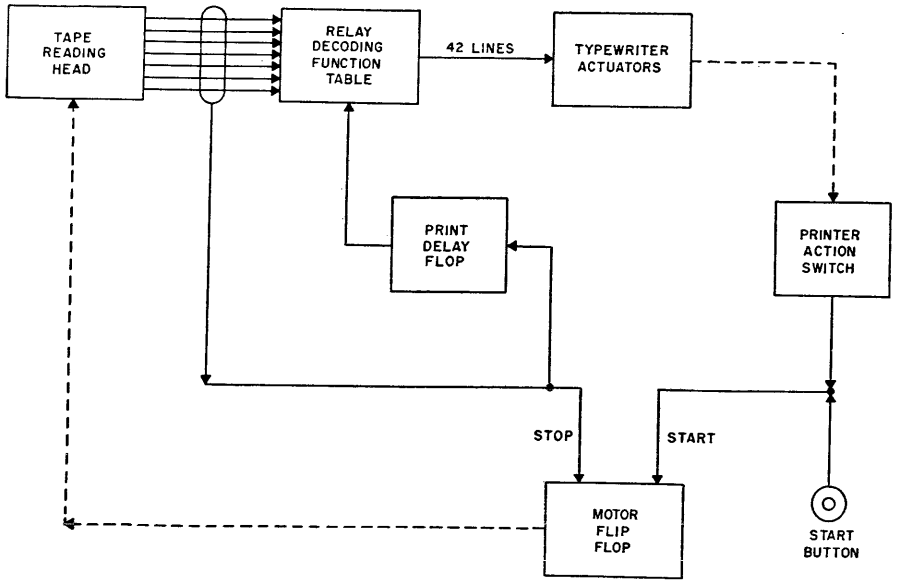

Figure 3. Simplified block diagram of Uniprinter

word-time is introduced to allow then function table signals to reach equilibrium. The time-out interval is controlled by a single fast-acting flip-flop. All gates attached to the function table signals which are critical as to opening and closing can be inhibited by the time-out flip-flop during time out. Regardless of the presence of the function table signals, the gate does not operate until the time-out flip-flop releases it. Thus, the burden of speed imposed by the short space between words has been shifted to a single flip-flop which can accomodate the needs of the entire computer.

The UNIVAC uses the excess-three pulse code system which requires a second binary adder after the main binary adder in order to provide the excess-three correction after each addition. On the other side of the ledger, the complementing operation for subtraction and division is very much simplified, since the substitution of ones for zeros and vice versa is sufficient to form a complement. The excess-three part of the pulse code occupies the four least significant digit positions. The next two positions beyond the excess-three digits are used as zone indicators. When these digits are both zero, the last four positions are interpreted as a numerical quantity; when nonzero, an alphabetic or punctuation symbol is indicated. The seventh channel is the check pulse channel.

The adder is provided with an alphabetic bypass circuit which allows an alphabetic letter to enter one input and emerge unscathed provided a numeral enters the other input. Thus additive numerical constants can be combined with instruction words to adjust the memory location part of an instruction without affecting the alphabetic instruction symbols.

The power supply for the computer is separately housed. It can be placed any reasonable distance from the central computer. Almost all rectification is done by dry disc rectifiers. The power supply provides all a-c and d-c potentials to the central computer, supervisory control, directly-connected printer, and the Uniservos.

A complete fusing system has been included which serves both as protection and as a short-circuit isolating means. Each section, of which there are 39, is locally fused, enabling the engineer to locate a short within only 12 chassis, rather than the total of 468.

An automatic voltage monitoring system may be used to test every d-c voltage at the rate of one per second. A meter movement relay signals any discrepancy from standard. Similarly, overheat thermostats detect any unfavorable temperature condition in the bays or mercury tanks.

Cooling for the power supply and central computer is provided by three blowers. Local cooling in the Uniservos is provided by small fans in each unit. The operating statistics of the UNIVAC are as follows:

Tape reading and recording:

Pulse density: 120 per inch
Tape speed: 108 inches per second
Input block size: 60 words; 720 characters
Tape width: 1/2 inch; 8 channels

Internal operations:

Memory capacity: 1,000 words; 12,000 characters
Memory construction: 100 mercury channels; 10 words/channel

Access time:

Average: 202 microseconds
Maximum: 404 microseconds

Word length:

12 characters
91 pulses
(include space between words = 7 pulses)

Basic pulse rate:

2.25 megacycles
Addition: 525 microseconds
Subtraction: 525 microseconds
Multiplication: 2,150 microseconds
Division: 3,890 microseconds
(All times shown include time for obtaining instructions and operands from memory)

Applications of UNIVAC

Types of Problems for Which UNIVAC Is Applicable

True to its name, Universal Automatic Computer, the UNIVAC system is capable of handling data processing or calculation in virtually all fields of human endeavor. It is particularly well suited to applications requiring large volumes of input or output data, or both.

For convenience and classification, applications of the UNIVAC will be treated under four headings: scientific, statistical, logistical, and commercial. The scientific problem usually, though not always, has relatively small amounts of input and output data, with emphasis on computation. The statistical problem has relatively large volumes of input data with a small volume of output data and simple processing procedures. The commercial and logistical problems both have relatively large amounts of input and output data with processing requirements varying from slight to relatively great. A number of problems in each of these four fields have been studied and found suited for solution on the UNIVAC system. Several in each field have actually been processed on the computer.

Scientific Problems

A general-purpose matrix algebra routine designed to add, subtract, multiply, and reciprocate matrices of orders up to 300 has been prepared and applied to a number of matrices. Inverses have been calculated for three different matrices of orders 40, 50, and 44. The error matrices for the first two of these inverses also

were calculated. In both, the largest error term was of the order of 10^{-8}. A triple product matrix was formed from component matrices ranging from 5 by 40 to 40 by 40. A check product was obtained by reversing the sequence of multiplications, verifying the original product to within 2 units in the 11th place. The computer time required for these calculations was 1 hour and 15 minutes to calculate the inverse of order 50, 45 minutes to determine its error matrix. The other calculations were proportionately shorter. In all of this work, magnetic tapes were used as temporary storage for the bulk of the matrix elements involved. The high speed of the tape reading units more than kept up with the computer's need for data. No mathematical checks, other than the over-all check mentioned, were included in the computation, the self-checking features of the system making these completely unnecessary.

A second computation—that of obtaining six different specific solutions to a system of 385 simultaneous equations—was completed in 27 minutes on the computer. The system of equations arose from a second order nonlinear differential equation of gas flow through a turbine. The error terms resulting from the substitution of the computed unknowns into the basic equation were of the order of 10^{-11}.

The third example is that of a 2-dimensional Poisson equation, using a 22 by 22 mesh. Each iteration required 13 seconds and produced a maximum separation of successive surfaces of the order of 10^{-8} after approximately 300 iterations.

Statistical Problems

In the second major field of statistical computation, the Census problem has been a prime example. The Census problem produces a part of the Second Series Population on Tables for the 1950 Decennial Census.

The Second Series contains 30 types of tables covering the statistics of our population—age, sex, race, country of birth, education, occupation, employment, and income. These tables are to be compiled for every county, and for every city, rural farm, and rural nonfarm area within a county.

The preparation of these tables by the UNIVAC system requires three major steps:

1. Tabulation of each individual's characteristics by groups of about 7,000.
2. Arranging these groups by cities, counties.
3. Assembling from the tabulations the data required for each table.

The raw data were prepared in the form of a punched card for each individual in the United States. The data from these enumeration cards are then transcribed onto magnetic tape. From these tapes, the computer processes the data sequentially through the three steps, producing output tapes from which the tables are printed on Uniprinters. The only manual operations encountered in this entire procedure are the handling of the original punched cards, mounting and demounting tape reel (the equivalent of 9,700 cards), and the removal of the printed tables from the Uniprinters.

The most important feature of the present procedure is the elimination of handling and sorting tremendous quantities of punched cards. Each handling of the card stacks is a source of potential error and delay. The UNIVAC memory permits the simultaneous accumulation of the 580 tallies which describe our population for each local area being studied by the UNIVAC system.

Commercial Problems

In the commercial field, the UNIVAC system has handled premium billing for a life insurance company. This program produces premium notices, dividends, and commissions. In a particular example worked out, approximately 1,000,000 bills, 340,000 dividends, and 100,000 commissions have to be produced monthly. The necessary information for processing a particular policy is contained in 240 digits, or, in special cases, 480. This compactness is made possible by a logical system of 40 symbols, comprising both alphabetic and numeric characters, which denote over 90 definitions. The UNIVAC processes the policies as directed by the symbols, policy dates, and policy numbers.

The problem includes inserting over 250,000 changes each month before further handling is done. After this step, the policies to be processed are selected from a file of 1,500,000 items. Next, a list is produced of the cases which have symbols indicating that special notices must be sent to the policyholders. Following the calculation of dividends and commissions, additional lists are produced: one group contains information pertaining to commissions and agents; another contains information regarding dividends; and finally, there is a listing of option changes for later insertion into the policy files. Policies requiring premium notices are then edited and the notices are automatically printed from the data contained on magnetic tapes.

The UNIVAC time needed for a program of this proportion is about 135 hours a month. The average computer time per policy processed is less than 0.5 second. The average time for all change insertions, printing, calculations, and unityping is 9 seconds per item.

Logistical Problems

In the field of logistics, five major studies have been conducted, four of these resulting in actual problems executed on the computer.

The first is the type of computation in which the basic purpose is to determine quantitively whether a given operational or mobilization plan can be logistically supported. The ultimate desired is to find, by calculation, the optimum program for carrying out such plans. At the time of writing, only a small model has been actually run on UNIVAC, but full size models will be run within the next few weeks. Two computations have been executed, one a set of three tables of thousands of lines each, giving a detailed breakdown of machine deployment, fuel requirements, and overhaul requirements. The other problem was a computation of the amounts of critical raw materials required to construct a given number of each type of equipment, these requirements being phased by quarters over a 2-year period. The fourth problem, which was actually computed, was a sample of a similar calculation in which every pound of critical raw material required each month for the ultimate construction of a complete building program was computed.

The UNIVAC program which was prepared is capable of accommodating every type of equipment, individually tailored construction schedules, detailed bills of materials running into the millions of items and of determining the actual amounts of alloy elements based on thousands of tables of percentages for the many alloys employed. The demonstration showed that this computation for 400 pieces of equipment of a given type could be executed in three hours of computer time. The last problem in this field has not yet been run, but the study has shown that the entire gamut of stock control for a large supply office can be covered by the computer in approximately 3 weeks time.

This program involves the maintenance of stock balances of hundreds of thousands of stock items for many service points and provides for the preparation of stock transfer orders, purchase requisitions, critical lists and summary reports.

Performance Record of the UNIVAC

Acceptance Tests

The Acceptance Tests, prepared jointly by the Bureau of Standards and Bureau of Census, are fully discussed in the following paper by Dr. Alexander and Mr. McPherson. However, a few comments concerning them from the engineering point of view are appropriate.

The Census computer was given two tests; the first, a test of its computational ability; the second, a test of its input-output system which particularly stressed the tape reading and recording abilities.

The Central Computer Acceptance Test A consisted of two parts. During Part 1, every available internal operation, except input-output operations, was performed. Among these operations were addition, subtraction, comparisons, division, and three different types of multiplication operations. Each of the arithmetic operations handled a pair of 11-decimal digit quantities. Altogether there were about 2,500 operations in the routine, yet the entire routine required only 1.26 seconds to do. The routine was performed 808 times in 17 minutes making a total of about 2,000,000 operations in all.

The second part of Test A included the solution of a heat distribution equation, a short routine involving the input-output device and a sorting routine. The sorting routine arranged ten numerical quantities each containing 12 decimal digits in correct numerical order in about 0.2 second. All three routines took a total of $1\frac{1}{2}$ minutes to perform. They were performed twice for each test and when added to Part 1 made a total of 20 minutes for unit test A.

The Acceptance Test B examined the input-output tape devices (Uniservos). During the first part of Test B, 2,000 blocks or about 1.4 million digits, which included every available character (numeric and alphabetic) were recorded on a tape and then read back into the computer with the tape moving backward. The information read back was then compared with the original data read out. The recording operation required about 4 minutes while reading back and comparison required about 8 minutes. The second part of Test B consisted of recording and reading over one spot of tape for 700 passes in order to determine the readability of tape as it wears. This test required 13 minutes and when combined with Part 1, made a total of approximately 25 minutes for Test B. This test was repeated 19 times.

The first test run passed in 6.6 hours (minimum theoretical time: 6.0 hours) and the second test was passed in 9.47 hours (minimum theoretical time: 7.45 hours). Of the 2.02 hours down time, 1.45 hours were accumulated at one time with the remaining 0.58 hours spread over the rest of the test.

The Uniprinter test required that a block of information (60 words) be printed 200 times in tabular form. The minimum time for printing was five hours. The test was passed in 6.16 hours.

The card-to-tape test required that ten good reels of tape be produced in 12 hours. There were certain restrictions as to reading accuracy and other criteria of reproducing ability which defined "good" reels. In 10 hours, the converter had prepared over 15 reels, 14 reels had been tested, 11 of the 14 were found satisfactory and the converter was accepted for payment.

Although the test was run on only one of two converters, the Bureau of Census put both card-to-tape machines into operation and after six months of use, the acceptance test was run on the second card-to-tape converter. This test differed to some extent from the first test in that the Census Bureau was satisfied with the reading ability of the machines and did not require a digit-by-digit verification of the information. However, a new stipulation was added that, after the engineers had checked the converter out preparatory to running the test, the converter was to be used in actual operation for eight hours before doing the remainder of the test with no engineering intervention between the two portions of the test. The first part was run on Friday, October 5, 1951; the device remained idle Saturday and Sunday and was turned on Monday morning to complete the test. It passed with flying colors, preparing ten acceptable reels (out of ten reels) plus two decks of check cards in slightly less than 7 hours. Both card-to-tape converters now are in Washington and the remainder of the system is in operation by the Bureau of the Census on the Eckert-Mauchly premises in Philadelphia.

Reliability and Factors Affecting Performance

The first UNIVAC system now has been operating for approximately 8 months. In that time, much has been learned about how UNIVACs should be operated and maintained. The situation has been somewhat complicated by having to shake down the equipment while in the customer's possession; that is, there were certain faults in the system from both engineering and production standpoints which could only become apparent in the course of time and under actual operation conditions. For example, weak tubes or faulty solder joints did not reveal their presence at the time of installation. Another type of difficulty only became apparent under certain duty cycle conditions imposed by various types of problems. Because only certain problems present this particular duty cycle, these troubles remained in the machine causing intermittent stoppages until they could be tracked down.

Patient isolation and elimination of such problems, most of which have occurred only with conditions of operation infrequently encountered, is a powerful, though sometimes painful proving ground for the engineering group charged with such responsibility. The experience and depth of judgment acquired by such a group in the course of performing such work have become unmistakably apparent in the already noted improved performance of following UNIVACs and generally advanced ability to predict and realize performance in any large scale and complex apparatus of the same character.

Some of the troubles encountered are interesting to study in detail. On a rather complicated routine requiring the use of a number of Uniservos, all ran smoothly for 15 minutes. At that time, one of the Uniservos executing a backward read somewhere in the middle of the reel, did not stop at the end of the block but continued to run until it ran off the end of the tape. After much work, it was shown that a cycling unit signal was being overloaded because it was being used both by a multiplication instruction and the backward read which were occurring simultaneously. The input precessor loop was cleared as a result and the count of the pulses coming off the tape was thereby lost. Once the trouble was found, it was simple to remedy.

Another rather interesting case occurred intermittently over an extended period. Normally when reading out of the memory, the contents should not be cleared. Occasionally, however, reading from the memory also caused the contents to be cleared. As the trouble only remained for a period of seconds or, at most, a few minutes, it was somewhat difficult to localize. Of course, parasitic oscillations of some sort were suspected and, in fact, the trouble was traced to the actual source on a logical basis; but the

source, a high power cathode follower, showed no evidence of oscillation. Before the problem was remedied, various combinations of parasitic suppressors were tried; the trouble would vanish for perhaps a week and then return. The oscillation finally cropped up during a maintenance shift, was found to be in the suspect tube at 100 megacycles and was eliminated rather easily.

Other types of troubles that have occurred include intermittent parasitic oscillations in other circuits, bounce in Uniservo relay circuits, various mechanical problems in Uniservos, time constants not consistent with the longest duty cycle signals, and various types of noise in the input circuits. The tubes, which initially were bothersome, have now stabilized to the point where two tubes per week (on the average) stop the computer during computation.

All of the above troubles and others not discussed here have contributed to lost computing time on the UNIVAC. However, they cannot influence future operation because the reasons for them have been found and eliminated. The fact that these troubles will not occur in future UNIVACs cannot be emphasized too strongly.

Under a contract with the Bureau of Census, Eckert-Mauchly Computer Corporation maintains the Census installation. This system is operated 24 hours a day, seven days a week, except for four 8-hour preventive maintenance shifts each week. This allows approximately 32 hours for regular maintenance and 136 hours for operation or 21 and 79 per cent respectively. Table I shows the engineering time spent on the computer system during typical weeks of operation. The figures are given both in hours and percentages. Both nonscheduled engineering time as well as preventive maintenance time are shown. The sum of the two gives the total engineering time spent on the computer per week. It should be noted that this is actual engineering time and does not include time that the computer may have been shut down while waiting for an engineer to report. According to our maintenance contract, this must be within a half hour during regular working hours and within two hours at all other times. Attention should be given to the fact that the preventive maintenance time does not total exactly 32 hours each week. This is due in part to a half-hour period each morning devoted checking and cleaning the mechanical portions of Uniservos. It is expected that this work will be taken over by the UNIVAC operators since the procedures and the techniques involved are quite simple.

Table I.

Week Ending 1951	Nonscheduled Engineering Hours	Nonscheduled Engineering Per Cent	Preventive Maintenance Hours	Preventive Maintenance Per Cent	Total Engineering Time Hours	Total Engineering Time Per Cent	Percentage of Nonscheduled Engineering
June 3	18.9	11.3	40	23.8	58.9	35.1	14.8
26	20.5	12.2	34	20.2	54.5	32	15.3
July 14	14.7	8.8	33	19.6	47.7	28	10.9
21	19.4	11.6	34.5	20.5	53.9	32	14.5
28	39.2	23.3	34.5	20.5	73.7	43.8	29.4
Aug. 4	26.2	15.6	33	19.6	59.2	35.2	19.4
Sept. 2	28.8	17.1	34.5	20.5	63.3	37.7	21.6
9	16.1	9.6	34.5	20.5	50.6	30	12.1
16	22.6	13.5	33	19.6	55.6	33	16.7
23	42.3	25.2	34.5	20.5	76.8	45.7	31.7
30	21.8	13.0	34.5	20.5	56.3	33.5	16.3
Oct. 7	15.9	9.5	56	33.3	71.9	42.8	14.2
14	14.0	8.3	34.5	20.5	48.5	28.9	10.5
21	10.4	6.2	34.5	20.5	44.9	26.7	7.8
28	20.8	12.4	33	19.6	53.8	32	15.4
Nov. 4	40.4	24.0	34.5	20.5	74.9	44.6	30.3
11	10.1	6.0	34.5	20.5	44.6	26.5	7.6
18	30.5	18.2	34.5	20.5	65	38.7	22
25	13.7	8.2	34.5	20.5	48	28.6	10
Dec. 2	14.8	8.7	34.5	20.5	49.3	29.3	12.6
9	19.6	11.7	34.5	20.5	54.1	32.2	14.7

In addition, one extra shift was required the week ending June 3 and three extra shifts the week ending October 7, 1951. These shifts were required to incorporate engineering changes which had been developed over a period of time and could not be incorporated in the equipment during the normal preventive maintenance time. The nonscheduled engineering time has varied from as little as 10.1 hours or 6 per cent to 42.3 hours or 25 per cent. The last column in the Table shows the amount of nonscheduled engineering time as compared to the allowable operating time (total time less preventive maintenance time). Here there is a variation of from 7.6 to 31.7 per cent and an average for the weeks shown of 16.9 per cent. It is believed that these figures, while good for the first months of operation of a new piece of equipment, will show definite improvement over the next year.

Although the opportunity to prove or disprove the following theory of operation has not presented itself, it is believed logical that optimum use of the UNIVAC equipment might be obtained by means of scheduling preventive maintenance only at such times as it is indicated in the judgment of competent operators. In other words, there are many occasions preceding a scheduled maintenance shift when the system is performing very well. At such times, it is extremely inefficient to shut down the operation in order to provide maintenance. For many reasons, however, it has been impossible to operate and maintain the first system in this way. It is hoped that such operation will be possible in following installations.

It should be realized that the UNIVAC system requires a supervisor of the same caliber as the one required for a large punched card installation. However, the large group of operating personnel would be replaced by a small group of well-trained extremely competent people thoroughly familiar with the details of the computer and associated equipment. The time spent in providing a high degree of training for these people is more than repaid in increased operating efficiency and consequently higher work output. For example, situations arise in the course of running a problem where a correct operational decision can save hours of elapsed computation. Also, a competent operator will recognize malfunctions sufficiently early to prevent serious delays. He is capable of deciding whether to continue with machine operation or to stop to diagnose. The second UNIVAC system which is ready for installation in Washington, will be operated by a group of engineers who have been trained in operation and maintenance. This procedure, it is believed, will result in the UNIVAC system being of maximum benefit to the Air Comptroller's Office.

Evaluation of UNIVAC Design

Checking Features

Maintenance of the UNIVAC has been vastly simplified by use of duplicate arithmetic and control equipment and other checking methods. Many factors which would have led to undetected errors have, by virtue of duplication, immediately stopped the computer. Al-

though checking by means of inverse operations can provide operational checks on the arithmetic circuits, there is some question as to whether it provides as good a check as duplication. However, in connection with odd-even codes, it may conceivably be comparable. It should be remembered, however, that this is from an operational standpoint and not a maintenance standpoint. When the control equipment is considered it is difficult to visualize a check that is as good as duplicated equipment. Other checks that are utilized in UNIVAC include the periodic memory check, intermediate line function table checker, function table output checker, memory switch checker, and 720 checker.

As explained earlier in the paper, the periodic memory check is accomplished by reading out of all memory channels sequentially and performing an odd-even check on each digit as it passes through the high speed bus amplifier. The period at which the check is repeated may be varied over a large interval. At present, it is set at 5 seconds, the check taking 52 milliseconds or about 1 per cent of the computing time.

The function table has a check at the very input by bringing in the check pulse in each character so that if an odd-even error occurs between the control register and the static register, no order will be set up and the computer will grind to a halt! If the input sets up properly but an error occurs farther on in the table, but not ahead of the intermediate lines (the linear set into which the input combinations are decoded), the error is caught at this point. The intermediate lines are broken into groups in such a way that an error is indicated when more than one line is set up in one group or the entire set. There is an exception to this in some groups where no error is indicated by this checker if more than one line is set up within the group.

This has been allowed only in those cases where it has been shown that setting up two or more lines will cause some other checker or checkers to indicate the trouble.

If the error occurs beyond the intermediate lines, the output checker then comes into play. This checker makes an odd-even count on the number of gates used on each instruction: dummy lines having been added so that the count is normally always odd.

The memory switch or tank selector checker ensures that one and only one memory channel is selected on any instruction. It checks each of the two digit positions separately indicating which if either, is in error.

The 720 checker counts the digits coming off the tape and if there are either more or less that 720 in one block, the computer stops; by examining the indicators on the supervisory control console, the operator can determine the number of digits actually read. By means of some rather simple manipulations, the operator can then reread the block without losing his place in the routine; and if the information is then read correctly, he may again start the computer on the routine. The same procedure may be followed if an odd-even error is made in reading from the tape.

Many checks other than those mentioned before have been built into the UNIVAC. On the basis of operating experience, the engineers cannot recommend too strongly the use of built-in checking facilities. All in all, the faith that can be put into results obtained from an unchecked computer comparable in size to UNIVAC is in the writers' opinion exceedingly low.

More than this, however, the methods by which the UNIVAC is checked have been of extreme usefulness in trouble shooting. The duplication of circuits has amply repaid the increase of space and the number of components required by this checking system.

General Comments

After evaluating UNIVAC performance over a period of eight months, the over-all picture of the UNIVAC design, in the minds of its designers, is extremely good. Certain phases of its design exceeded expectations, while of course, other phases were somewhat disappointing. The first eight months of actual operation have taught more than years of experimentation with laboratory models. Many improvements have already been conceived of this experience and are continuing daily to increase reliability.

The other major factor influencing computer design, cost, has been duly considered in the UNIVAC design; and it is being met with plans for a continuing full-scale production of UNIVAC systems. As the production techniques are developed concurrently with the engineering design details, the UNIVAC becomes the realization of a hope which has long been in the minds of its designers: An economical, completely reliable commercial computer for performing the routine mental work of the world much as automatic machinery has taken over the routine mechanical work of the manufacturer.

Discussion

W. P. Byrnes (Teletype Corporation): At what speed does the input read from your magnetic tape into your input register?

J. R. Weiner: The tape moves at approximately 100 inches per second, and we record a pulse density of approximately 100 decimal digits per inch. I say "approximately" because as long as the machine dumps the decimal digits out at a rate corresponding to that product, it does not make much difference at what speed the tape runs. In other words, if we vary the tape speed from 100 inches per second to 120 inches per second, or vice versa, but continue to read the information out of the machine onto the tape at the same speed, we would read back into the machine at that speed.

J. L. Hill (Engineering Research Associates): Would you mind summarizing your experience with germanium diodes?

J. R. Weiner: Not at all. We have had excellent experience with them. We have found that most of the trouble encountered has been due to the engineers doing such things as short-circuiting voltages to ground with screw drivers and so on and damaging crystals accordingly. We check all crystals in the machine approximately every three or four months; we have found very, very few failures, and we have approximately 18,000 of them in the machine. In almost every case we have been able to trace a failure to an accident.

While we are waiting for another question I would like to add that one thing I did not cover in the paper is the fact that all the arithmetic equipment in the machine and most of the control equipment is duplicated. In addition, we run a continuous check on the contents of the memory, checking the entire contents approximately once every 5 seconds, and therefore we do not need any program checks.

L. A. Ohlinger (Northrop Aircraft Company): Would you clarify one thing about what you said of input and output of the single word? Do I understand you can enter a single word at any chosen position in the memory and remove that word without interference to the rest of the information in the memory?

J. R. Weiner: That is right. We can do that in a number of ways. If we stop the machine, we can empty from any position in the memory by use of the supervisory control facilities. We can also type into any position of the memory and do either of these without interfering with the routine that is already in the memory. Once we do this we can start the operation again. We can also program the problem in such a way that it will automatically print out the contents of specified memory locations at

specific points in the routine, or it will stop and wait for the operator to type in a number before it continues.

L. A. Ohlinger: Does that make it possible to replace a single word, are in effect erase the word and substitute another word?

J. R. Weiner: Very definitely. And incidentally, it has proved to be a very useful facility on many problems.

J. Naines (Northwestern University): Have you made use of transistors in UNIVAC?

J. R. Weiner: No. We have approximately 5,000 vacuum tubes in the UNIVAC, 18,000 crystals, and no transistors. About the time UNIVAC was started, which was approximately four years ago, there were no transistors available.

Dr. S. N. Alexander (National Bureau of Standards): I would like to point out one thing about the maintenance experience of the UNIVAC.

We tried to set it up so that the maximum possible useful time would be available to Census, and no holds were to be barred, including such things as borrowing spare chassis out of Machines 2 and 3 which were in production. Therefore, this represents an advantage which will not be available when the baby is taken home.

However, I think that this is not to be construed as criticism. It is just indicating that when you are trying to get Number 1 going, you will do anything possible to keep it going and learn what it is you need to fix in the machine in order for it to stand on its own feet.

I would also like to point out that the maintenance people available for this job are probably the peak quality personnel that will ever be allowed to maintain one of these machines. When it is maintained by the designers it gets a loving care that it will probably never receive again.

For this reason I would like to point out that you must weigh these facts with the records ascertained, trying to balance out how much this offsets the fact that it is Machine Number 1 which we are trying to learn a great deal about.

I hope the records on Machine Number 2 will become available in which it will be operated and maintained by people away from the plant but who have been trained at the plant by the Eckert-Mauchly personnel.

Would you care to add anything to that, Mr. Weiner?

J. R. Weiner: I would like to say that I agree with everything that Dr. Alexander has said. However, I would like to add a few comments.

The first UNIVAC was the first machine of its type and a rather ambitious machine. Although we have time listed which we call preventive maintenance time, a good bit of that time has been spent in hunting troubles down, and once they were hunted down and fixed they were troubles that would not recur in later machines; this has proved true on UNIVAC Number 2. We have not had the trouble on Number 2 that we had on Number 1. I would say also that perhaps 80 per cent of our time on Number 1 has been spent in trying to get input-output operation as reliable as computer operation, operation that would completely satisfy Dr. Alexander. I feel that we have probably succeeded in doing that to a very great extent on Number 2.

I certainly agree that you do not want to use $10,000-a-year engineers for maintaining UNIVAC, and I do not think we will. I would say the troubles we have had on Number 1, and we have had many, are not at all representative of the sort of thing you would expect on later machines.

B. V. Bowden (Ferranti, Ltd., England): I would like to ask what sort of magnetic tape you use in the memory?

J. R. Weiner: We use metal tape of our own manufacture. At the time we started working on UNIVAC, there was no tape available that we felt was sufficiently reliable, and we started our own tape development program. I think we were very fortunate in doing that. The tape is metal base and we put a magnetic plating on it. We do have pin holes, and other defects in the tape but we take care of them by punching out the occasional bad spots on the tape, before the tape gets to UNIVAC. In other words, we inspect every reel before it is used, punch out the bad spots and detect them automatically on UNIVAC, and do not write on those portions of the tape or read from them. We find that this procedure has worked out quite well.

Performance of the Census UNIVAC System

J. L. McPHERSON S. N. ALEXANDER

In June of 1948 the National Bureau of Standards acting on behalf of the Bureau of the Census contracted with the Eckert-Mauchly Computer Corporation for a UNIVAC System. This UNIVAC System, now generally known as the Census UNIVAC System, was accepted on March 30, 1951, and since that time has been devoted almost exclusively to tabulating results of the 1950 Census of Population and Housing.

We will try to present here certain facts about the acceptance testing and about operating experience. We also will indicate the inferences we have drawn from these facts. We are aware that any given body of facts may be, and often is, interpreted in a variety of ways depending upon just what it is that the interpreter is trying to prove. We will try carefully, therefore, to distinguish between our facts and our inferences. Furthermore, we will try to present the extremes of the conclusions that might be drawn from the facts. One of your authors is an engineer with some familiarity with the difficulties of physically realizing the grand promises frequently made for, and not always by, engineers. Your other author is in the business of producing statistics. He is interested in any tool that will increase the efficiency with which he conducts this business. For purposes of this paper, at least, each of us will do his best to be a good advocate for his devil.

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Acceptance Testing

At the time it was accepted the Census UNIVAC system consisted of a UNIVAC computer, four Uniservos, a Uniprinter, and a Card-to-Tape Converter. The question of the acceptability of this system was a difficult problem. Our contract for a UNIVAC System specified a variety of operating and performance characteristics, such as the instruction code, the execution time for each instruction, and the required tape speed in characters per second. However, we quickly decided that to test specifically for each of the detailed facilities required by the contract not only would be extremely difficult to plan and to monitor but also would provide information beyond our ability to interpret.

We wanted a device to do Census work. If there was a high probability that the

UNIVAC would do Census work efficiently we wanted to accept it and if not we wanted to reject it.

At the time the UNIVAC system was submitted to the government for acceptance testing the only significant problem we had programmed for it was the tabulation of the Second Series Population Reports for the 1950 Census of Population. This program had never been used by the UNIVAC. It was not "debugged." For this and many other reasons it was not a suitable program to use for acceptance testing. However, its existence enabled us to estimate a statistic which proved very useful in designing an acceptance test. This statistic was the time it should take the UNIVAC to tabulate the Second Series Population data for one reel of population information. Our estimate was 20 minutes. (Later experience indicated that the actual average time per reel for this problem is 19.6 minutes.)

We must admit that we did not realize the importance of this 20-minute figure until we had explored several lines of approach to an acceptance test for the central computer. We had great difficulty in deciding just what would be a reasonable upper bound to set on the number of wrongly executed instructions per million. Moreover, we found that it was by no means easy to decide how we would go about determining how many orders the machine had wrongly executed, if any, in the course of a program.

We spent a considerable amount of time fruitlessly searching for a way to get to the heart of this problem. Then, happily, we sought the advice of Dr. Joseph F. Daly, Chief of the Statistical Methods Section, at the Bureau of the Census. He pointed out that the important consideration was not how many errors the machine made when things went wrong, but rather, how often it could be depended upon to get through a problem correctly. With Dr. Daly's help we finally concluded that what we wanted was a machine which would be fairly certain to operate satisfactorily throughout any given 20-minute running period. In addition, we felt that it would be reasonable to accept a machine which would be in operation at least 50 per cent of the time; for we assumed that if the computer had the required reliability, the problem of keeping it in operation most of the time would be mainly a matter of gaining experience in maintenance.

In order to arrive at a set of numerical specifications for the test, we took over one of the standard sequential sampling plans, using the 20-minute problem as a sampling unit. Since we could not take a random sample of such 20-minute units, the probabilities associated with the plan were perhaps not too meaningful. Nevertheless, it may be of some interest to note that if the chance that the machine would get through any particular 20-minute run was independent of its chances of getting through any other 20-minute run, then the plan had the following characteristics:

1. If the machine was such that on the average it would get through 90 per cent of its 20-minute problems successfully, the test would be almost certain to accept it (the chance of rejection being only 1 in 100).

2. If the machine was such that on the average it would get through only 70 per cent of its 20-minute problems correctly, the test would be almost certain to reject it (the chance of acceptance being only 1 in 100).

We prepared two routines to test the central computer. One of these was to test internal computation ability and the other was to test the communication between the computer and the magnetic tapes. Each of them was timed to require 20 minutes to complete. The following abstract from the acceptance test procedure for each of these two tests indicates the manner in which they were conducted:

"The test shall be rated as 'passed' if at the end of any test unit:

1. The 'down time' does not exceed the 'running time' and simultaneously:

2. The number of completed test units with one or more major defects does not exceed 0.186×(number of units completed) minus 3.41.

3. The number of completed test units charged with minor defects does not exceed one third of the total completed test units.

"The test shall be rated as 'failed' if at any time the number of completed test units with one or more major defects exceeds 0.186 × (number of units completed) plus 3.41."

Major and minor defects were defined in the test rules. "Down" time was defined as "total" time minus "running" time; and "running" time was computed by multiplying the number of completed test units by 20 minutes. Thus the UNIVAC was credited with having operated successfully for 20 minutes each time it produced an error free unit regardless of how long it might have taken to complete that unit.

In addition to the two tests of the central computer we designed a test for the Uniprinter and a test for the Card-to-Tape equipment. We will say more about them shortly. First we want to report on the performance of the central computer during the two tests applied to it. Certain calculations concerning the duration of these two tests can be made. These are:

	Computer, Hours	Communications, Hours
Minimum time possible to pass	6	7
Expected or average time to pass if 90% successful	9	10½
Expected or average time to fail if only 70% successful	7	8
Probable maximum length of test	25½	30

The test of computation ability was passed in 6 hours and 36 minutes, the test of communication between the computer and the magnetic tapes was passed in 9 hours and 28 minutes. One of the 18 test units successfully completed during the test of computational ability was charged with a minor defect. According to the test rules there could have been six units so charged. The test of the communication between the computer and the magnetic tape terminated with six of the 19 successfully completed test units charged with minor defects.

The Uniprinter test required a block of 60 words of information to be printed not less than 200 times. The constants in the formula for the Uniprinter test were such that we would be almost sure to accept a printer that would print 95 per cent of the 60 word blocks perfectly and almost sure to reject a printer that would print only 90 per cent of the blocks perfectly. Here the time computations indicated the following:

	Hours	Blocks
Minimum possible time to pass (1.5 minute units)	5	200
Expected or average time to pass if 95% successful	7	274
Expected or average time to fail if only 90% successful	5½	216
Probable maximum time	14	566

This test was passed in 6 hours and 10 minutes.

For the Card-to-Tape equipment we decided that a device capable of successfully transcribing the information from punch cards to magnetic tape at an average rate of 70,000 cards per 8-hour shift would be satisfactory. This converts to about ten good reels of tape every 12 hours. There were necessarily two phases to this test. First the cards had to be

run through the converter to produce the tape. Second the tape had to be run through the UNIVAC to determine whether or not it was satisfactory.

According to the conditions we established for this test it was necessary that the Card-to-Tape equipment produce ten "satisfactory" reels in 12 hours. The manufacturers were permitted to prepare as many reels as they could during the 12 hours. It was up to them how much time was spent running cards through the machine and how much time was spent making any adjustments they felt were needed.

It was not necessary for a reel of tape to be perfect in every respect to be satisfactory. There are two types of errors that the Card-to-Tape equipment can make.

1. It can record on the tape the pulse pattern for a character (or combination of characters) which is readable by the UNIVAC but which does not represent the character (or combination of characters) which appears in the punched card being transcribed.

2. It can record on the tape a pulse pattern which the UNIVAC cannot interpret. The check circuits in the UNIVAC are such that it stops when it encounters a pulse pattern it cannot interpret.

A satisfactory reel might contain a small number of the first type of errors but it could not contain any errors of the second type.

After 9 hours and 55 minutes of operation and maintenance the Card-to-Tape device was preparing the 16th reel. By then 14 reels had been tested by the UNIVAC and 11 of them were found to be satisfactory so the test was "passed."

Let us now recapitulate the results of the four tests. The UNIVAC passed the test of computing ability with ease. It passed the tape reading and writing test, but by no means as easily as it passed the computing test. The Uniprinter test and the Card-to-Tape test were both passed quite satisfactorily.

We were (and we are sure the manufacturers were) pleased and encouraged. We gladly accepted the UNIVAC system and proceeded to put it to work on Census tabulations as rapidly as possible.

Operating Experience

The Second Series Population Reports problem, which was the problem we thought we were ready to start on the UNIVAC, consists of four main parts. We call these parts: tallying, merging, dispersion, and summarizing. Each is a separate entity in the sense that each consists of a program of instructions recorded on a separate instruction tape. Furthermore, the output of the tallying is the input for the merging, the output of merging is the input for dispersion; and the output of dispersion is the input for summarization. The outputs of summarization are the Census tabulations we want to publish. Although these parts are separate and distinct they do not account for equal amounts of UNIVAC time. The tallying part is far and away the most time consuming. At least four or five times as much UNIVAC time is required for tallying as for the other three parts combined.

In the preceding paragraph we said we thought we were ready to start this problem when we accepted the UNIVAC system. More precisely we thought we were ready to start the tallying part. As it turned out, the program of instructions for this part contained a few errors and it was not until approximately a week after we accepted the UNIVAC that we had a corrected program and were actually "in business." Filled as we were with high hopes and expectations the week we spent in getting the last bug out of our instruction program was an investment we hated to have to make. Our patience wore thin. Like children at the circus we could not wait for the show to start. Now, about 8 months later, we are years and years wiser. Now we recognize what a phenomenally good job we had done preparing that program. We doubt that ever again will we be fortunate enough to succeed in debugging a program as complicated as our tallying routine in as short a time as one week.

By the middle of April 1951 we knew we had a tallying program that worked and that we had some employees who knew how to use it. These people, however, were skilled programmers. We needed their service to complete the programs for merging, dispersion, and summarizing and to develop programs for other Census work. For several weeks before we accepted the UNIVAC we had been training people to be UNIVAC operators but they had had no practical experience. Since the UNIVAC we accepted was the first one in the world and because right up to the time we accepted it the engineers who built it had been working on it, our operators had never manipulated the controls of a UNIVAC until they were taught how to run our tallying routine. We were pleased with the rapid progress these operators made. By about the middle of June we had enough confidence in them that we felt they could operate the UNIVAC without the supervision of a programmer. We then began full time operation, 24 hours per day, 7 days per week. Four 8-hour shifts per week the UNIVAC has been assigned to engineers for preventive maintenance. The rest of the time we have been operating it except for those times when a malfunction necessitated emergency maintenance.

One of the responsibilities of our operators is the maintenance of a log in which they must account for every minute. We have been quite satisfied with the way our operators have kept this log. In fact their ability to keep it has somewhat exceeded our ability to digest it.

We have summarized and analyzed the log for about 85 per cent of the period beginning June 20 and ending October 28. The missing 15 per cent consists of a few days early in July and a few days early in August. To the best of our knowledge and belief there is no reason to think UNIVAC performance was any different during these periods from its performance during the periods for which the log has been summarized.

We do not have time to present our summary and analysis in complete detail. Therefore, we will concentrate on just one phase of our analysis, namely the proportion of the time the UNIVAC has been useful to us. Remember we have been on a 24-hour-per-day 7-day-per-week schedule. Table I, "Summary of Census UNIVAC Log," provides practically all of the numbers necessary to follow our analysis.

The conclusion, most favorable to the UNIVAC system, that can be drawn from these data is that it was "available for use" 59 per cent of the time. This is an important statistic and we are

Table I. Summary of Census UNIVAC Log

June 20 to 26, July 8 to August 4, August 13 to October 28, 1951

	Minutes	Per Cent
Total in period	161,280	100.0
Regularly scheduled preventive maintenance	32,872	20.4
"Down"	33,667	20.9
Tallying	37,823	23.5
Success (945 reels)	23,499	14.6
Failure (723 reels)	14,324	8.9
Equipment fault (569 reels)	10,687	6.6
Census fault (131 reels)	2,854	1.8
Unknown (23 reels)	783	0.5
Salvaging	18,547	11.5
Success (497 reels)	11,745	7.3
Failure (329 reels)	6,802	4.2
Other*	36,854	22.9
Unexplained	1,517	0.9

* Other time includes time spent on merging, dispersion and summarization; time spent "proving in" routines, time during which problems other than the Second Series Population Reports were being run, time during which the UNIVAC was loaned to non-Census users.

encouraged by it. Remember for our acceptance test we had decided that a device which could be operable 50 per cent of the time would be useful to us.

Another conclusion, not nearly so favorable to the UNIVAC system, that also can be drawn from the same data, is that it was "useful" only 28 per cent of the time. This is probably at the extreme low end. The true measure of utility of the system during the period analyzed undoubtedly falls somewhere between 28 and 59 per cent.

The 59 per cent "available for use" is obvious from the table. It is "total time" minus the 20.4 per cent of the time allotted to regular preventive maintenance and the 20.9 per cent of the time spent on emergency maintenance.

The 28 per cent "useful" time requires some interpretation of the data shown in Table I and some estimates based on these interpretations. These are summarized in Table II.

Table II

	Total, Minutes	Useful, Minutes	Lost, Minutes
Successful tally	23,499	18,900*	4,599
Tally failure, equipment fault	10,687	.....	10,687
Tally failure, Census fault	2,854	2,854	....
Tally failure, unknown fault	783	783	....
Salvage	18,547	3,951**	14,596**
Subtotal	56,370	26,488	29,882
Subtotal, per cent	100.0	47.0	53.0
Other and unexplained	38,371	18,034†	20,337†
Maintenance	66,539	.....	66,539
Total	161,280	44,522	116,758
Total, per cent	100.0	27.6	72.4

* 945 reels at 20 minutes per reel

** Of the 723 reels which failed on tally, 154 or 21.3% were not definitely attributable to equipment fault; here 21.3% of the time spent salvaging is classified as useful.

† Here the 38,371 minutes in the total column is distributed between useful and lost in the same proportion as the preceding subtotal.

Before we enter numbers in the "Useful" and "Lost" columns let us briefly describe a preliminary operation involved in the preparation of the Second Series Population Reports. The Census information for each person is recorded on a punch card. Before we can use the UNIVAC we must transfer this information to magnetic tape using the Card-to-Tape converters. One reel of tape accomodates slightly less than 10,000 punch cards. After the data has been recorded on tape we start the tally, merge, disperse, summarize sequence described earlier.

During the period on which this analysis is based we attempted to tally 1,668 reels. This tallying process accounted for approximately 22 per cent of all the time being analyzed. We succeeded in tallying 945 of the 1,668 reels and failed on the remaining 723. We will say more about the failures presently. First let us make a few comments about the successes. We know that if the UNIVAC functions properly in all respects it requires 20 minutes to tally a reel of data. At this rate the minimum time in which we could expect to tally 945 reels would be 18,900 minutes. Actually we spent 23,500 minutes on these reels. What caused this difference of 4,600 minutes? The explanation is that during the course of tallying some, but by no means all, of these reels the UNIVAC malfunctioned. For example, our log might show that 10 minutes after a given reel was started on the tallying process the UNIVAC failed and it was necessary to call a maintenance engineer. The 10 minutes was lost. After the UNIVAC was repaired it still took 20 minutes to tally that reel.

Now what about the 723 reels we were unable to tally. Our log is ambiguous about why 23 of these failed. For 131 of them the failure could be attributed to a mistake made by Census personnel. For example the Card-to-Tape operator may have fed the punch cards upside down. The failure of 569 reels we classified as "equipment fault." By this we mean that somewhere along the line the UNIVAC system failed. A typical case is the one where the tallying operation proceeds for several minutes, perhaps 12 or 15, and then the UNIVAC stops because it reaches a section of the input tape it is unable to read. This may be because the Card-to-Tape device malfunctioned when the cards were recorded on tape. It may be because the Uniservo on which the tape is mounted is not functioning properly. We believe, and we think the Eckert-Mauchly Company people agree with us, that malfunctioning of the Card-to-Tape equipment was responsible for most, but not all, the tally failures attributable to "equipment fault." In September the company made some changes in the Card-to-Tape which we, and they, hope will improve its performance significantly. As of October 28 it was not possible to say with assurance that these changes were beneficial but what little evidence was available indicated that they were.

We spent something over 14,000 minutes trying to tally reels on which we eventually failed. Of this 10,687 minutes was spent on the 569 reels which failed because of incorrectly operating equipment. This time was just as real a loss as the time the UNIVAC was not available for our use.

Perhaps here is the place to interpolate some comments about UNIVAC tape reading and writing. There are approximately 1,000,000 characters recorded on each full reel produced by the Card-to-Tape device. To the best of our knowledge UNIVAC tape reading (and writing) speeds are at least twice those which have been attempted for any other computer. The UNIVAC reads tape at 10,000 characters per second. Here, then, is a requirement for an extremely high order of accuracy. The error frequency must be less than one in a million before we can successfully tally a reel. From the engineer's point of view the 945 reels that were tallied successfully are testimony that important progress in tape recording has already been achieved. From the user's point of view the 569 reels which were not acceptable to the UNIVAC represent a challenge to engineers to improve still more the fidelity of tape recording. To the engineers, we say that this may be the area in which the most important contributions can be made toward maximizing the usefulness of electronic computers for handling large masses of input, intermediate, and output data.

What do we do about reels we are unable to tally? At first we did the obvious thing; we reran the cards through the Card-to-Tape, device preparing new reels in the hope that we could successfully tally them. Then we decided to develop a program we called our "Salvage" routine. This was a routine to use the UNIVAC to reproduce the good parts of defective reels. It depended on the operator to substitute good information for the bad parts of defective reels.

The rules under which our operators worked this routine were technical and complicated. We will not go into them here. It will suffice to report that during the time we are analyzing there were 826 reels attempted on the "Salvage" routine. We succeeded in salvaging 497 of these and failed on the other 329. Here a success is the creation of a new reel that can be used as input for our tally routine. A failure represents a decision on the part of the operator that he cannot create a new reel without violating the rules relative to substitution of good information for bad.

It takes an average of 45 minutes to run a reel full of data on the Card-to-Tape device. When we introduced the Salvage routine we hoped we would get

tallyable reels with a smaller investment of time than would be required if we reran at Card-to-Tape each reel which failed on the tally routine. As it worked out we did not save nearly as much time as we had hoped. It would have taken 37,170 minutes to rerun 826 reels on Card-to-Tape. We spent 11,745 minutes successfully salvaging 497 reels. In addition we spent 6,802 minutes on the 329 reels we were unable to salvage. These 329 reels had to be rerun on Card-to-Tape which required 14,805 minutes. Thus we spent a total of 33,352 minutes on these 826 reels which is about 4,000 minutes less than would have been required if we had not introduced the salvage operation.

This saving is about 10 per cent, which while it is not trivial, is significantly less than the 40 to 50 per cent saving we had hoped for.

As far as the UNIVAC itself was concerned the time spent on this salvaging operation was something we had not originally contemplated. In a sense that time is lost even though it does not appear in "down" time. If reels had not failed during the tallying operation there would have been no need for the salvage process. It would be unfair to the equipment to charge it with all the time spent salvaging because our own errors were responsible for our inability to tally some reels. However, since 78.7 per cent of the tally failures were because of equipment fault we may be justified in saying that 14,956 minutes spent salvaging was lost to us as far as the production of population statistics was concerned. Much of this lost time is chargeable to faulty recording by the Card-to-Tape device.

Now we can accumulate the "Useful" and "Lost" time for these items which are those for which our log is reasonably specific. These subtotals indicate that 47 per cent of this time was useful and the balance was lost.

At this point we can use these percentages to classify the "Other" and "Unexplained" time. We realize that this is quite arbitrary. It certainly can be argued that this overstates the "Lost" time because of the inclusion, in the total 38,371 minutes, of time spent "proving in" routines. We are, however, attempting to develop a lower bound for our measure of utility and in that light we believe this is justified.

Finally we add the maintenance time.

Now the totals indicate that 27.6 per cent of the time was "useful" and the balance was "lost." This then is how we estimate the lower or our two percentages. The truth undoubtedly lies somewhere between 28 and 59 per cent.

One very important general comment should be made before we conclude this paper. It is that we cannot point to a single case where we can say with certainty that our UNIVAC system produced a wrong answer that could be traced to malfunctioning of the equipment. The error detection circuitry prevents this. When a malfunction occurs the UNIVAC stops and refuses to deliver any answers. It just will not deliver wrong answers.

We have had our troubles with our UNIVAC; we have lost patience with it many times; we have learned that we have very much to learn about how best to use it; and we have learned that the engineers have very much more to learn about how best to maintain it. We have on occasions been quite disappointed. But we have not been, and are not discouraged.

We are currently planning work which we believe will keep our UNIVAC system busy until the fall of 1952 at which time we expect to move it to Washington. Our estimates indicate that at its present levels of performance our UNIVAC system will accomplish this work at about one half the cost of doing it with any of the other tools which are available to us.

Discussion

J. W. Carr (MIT): Have you planned any programming so that you can process your log data itself? It would seem that possibly that would aid in producing statistics.

J. L. McPherson: The answer is no. We have found that programming time is at a great premium. I think that it is an interesting suggestion. The log is not a very orderly thing. Personally I would hesitate to try to program the summarization and analysis of it because I think it would be a job. I do not think it would be impossible by any means. We do not feel that we can turn our resources to that sort of thing with all the census work that is waiting to be programmed.

E. C. Berkeley (Edwin Berkeley and Associates): In your chart (Table I) of the use of UNIVAC time you show 22.9 per cent of time spent on other problems, including time during which the UNIVAC was loaned to noncensus users. On what basis is UNIVAC loaned to noncensus users who can use UNIVAC?

J. L. McPherson: Maybe this was just a fancy way of saying, "loaned to the manufacturer." Most of this was time that the Remington-Rand people were using the machine in accordance with an arrangement we made with them. This was in return for some programming assistance that they gave us. These people deserve a certain amount of sympathy. They worked, sweated, and slaved to produce a UNIVAC that operated. Finally they did, and along we came and accepted it and they did not have one. This is a situation which the company seems to be repeating.

In addition we have, as a part of the Federal Government, felt a certain responsibility to other parts of the Federal Government to let them try problems on our UNIVAC for purposes of evaluating it for their work.

I think it is correct to say that the only noncensus users have been either the Eckert-Mauchly programmers themselves, in accordance with our barter arrangement, or other Federal agencies which have made arrangements, generally with me, to get small amounts of time to try UNIVAC out on test problems.

A. Wertheimer (Navy Department): You said you estimate that the cost of using the UNIVAC will be about one-half of any other means. Can you tell us what you estimate it will cost you to maintain and operate the UNIVAC in Washington, if you can include also all appropriate costs, like the coders, operators, maintenance men, and so on?

J. L. McPherson: About $20,000 a month is what we are estimating.

L. A. Ohlinger (Northrop Aircraft Company): I would like to ask how many programmers and coders are employed in order to keep UNIVAC busy full time?

J. L. McPherson: We do not distinguish between programmers and coders. We have operators and programmers. You must remember the census job is such that once you have a program, you keep the machine busy on that one program for months. We have five operators and, I think, eight programmers.

P. C. Rapp (Bell Aircraft Corporation): I would like to ask if you have tried to do more or different things in view of the availability of the computer than you would have done with just punched card equipment?

J. L. McPherson: Yes, indeed. On this job that we are doing now, Second Series Population Reports—the proceedings of the meetings of the Association for Computing Machinery at Aberdeen about three years ago include a paper that tells how we carry this process much further with UNIVAC than we can carry it with punched cards.

The UNIVAC output, a sample of which you saw on one of Mr. Weiner's slides of a table showing population statistics classified by color, sex and age, is arranged almost exactly as we want to publish it. The punched card techniques we use do not usually provide the statistics in that arrangement.

If I can talk about the table Mr. Weiner projected for a minute–there were seven columns on that table namely (1) total both sexes, (2) total males, (3) total females, (4) white males (5) white females (6) nonwhite males (7) nonwhite females. I do not remember exactly how many lines there were on the table but the first few were (1) total

(2) under five years of age, (3) under one year (4) one or two years (5) three or four years. The UNIVAC output provided numbers for all columns and all lines. The punched card techniques we use would supply numbers for only the fourth through the seventh columns and the third through the fifth lines. We would have to compute manually the numbers for the other columns and lines. I do not want to say punched card equipment is incapable of producing an output as satisfactory as UNIVAC output, but it is true that using the abilities of the people we have at the Census we have not devised ways to get this kind of output from punched card equipment and we have obtained such output from the UNIVAC. We do not know how to do it using the punched card equipment and do it economically. So we feel that we are not only replacing a lot of punched card equipment but a lot of clerical work in the computation of derived statistics which has to take place when we use the punched card equipment.

W. H. MacWilliams (Bell Telephone Laboratories): Two questions about the salvaging in your table. I do not quite understand the basis of it since if you add the successful reels, 497, and the failures, 329, you come out with a larger number than the failures that you had to start with, 826 as compared to 723; and second, what was involved in the 329 reels that were failures to the end? Were you able to reprocess them or did those people just not get counted?

J. L. McPherson: As to the first question, this, I think, is simply because of the incompleteness of the time period. You should not expect the number that we tried to salvage to equal the number that we failed to tally. Some of these we tried to salvage could have been tally failures that occurred either prior to June 20, or during any one of the periods that are not accounted for, or it could be the second, third, or fourth attempt to salvage the same reel.

On the second point, I think all I can do is define successful salvaging. Successful salvaging is the creation, at the UNIVAC, of a reel which we then try to tally; whereas a failure in the salvage operation represents a decision that we must go back to the card to tape equipment and rerun the cards from which that reel was originally prepared. This decision is reached in terms of technical rules that we supply our operators.

J. B. Lindon (Consolidated Edison Company of New York, Inc.): Assuming that you initially punch the cards manually, assuming further that you did not have the cards and you were going directly to the tape, what factor of error do you think you would obtain? Also what factor of error exists between the cards and the tape?

J. L. McPherson: We have very little evidence on which we can base an answer to the first question. We have gone directly from manuscript to tape only in the case of our programs, using the Unityper that was described. We find on the average one out of every 60 words will contain an error. A word is 12 characters. So this is one error in 720. We have told our operators who are doing this transcription to be extremely careful. I think we are getting something like four or five times this 720 per day which, if I can do some very quick mental arithmetic, would convert to something like the information for 30 people recorded on tape per operator per day. For 150,000,000 persons, it would take the Defense Budget to pay the operators, and we would still have every sixth person with an error.

The evidence we have with respect to the use of the card-to-tape equipment is that it makes practically no errors of commission. In our acceptance tests we were willing to accept a rate of $1^1/_2$ errors per thousand cards. We were well below that. I do not recall ever seeing any statistics that would indicate that it was making more than about 12 errors per thousand cards, and this was when we thought that the equipment was in pretty bad shape.

J. B. Lindon: Could we assume that you could safely impulse a tape from a card, store it away for some length of time, and then dig it out and process it? That is to say not process it immediately—say you had some statistical information that it was not imperative to process, you could defer processing it, would you have sufficient confidence in the card to tape impulsing to put it off, say, for six months of a year?

J. L. McPherson: Well, we do. We do not like to have to wait those times in some of this work, but we actually are just now getting around to making the second use of some information that we recorded on tape and used for the first time six and seven months ago.

J. L. Lindon: Would it not be true that samplings, instead of making the complete run of statistics, may reveal the information you want. That is to say, you would accumulate it on the tapes but only use it as conditions warrant supplying the information.

J. L. McPherson: Well, this sounds like a Utopian kind of Census life that a lot of us would like to lead. Many of us think we could use samples to provide a lot of information, but we do not feel that this would be generally acceptable to the public on the one hand, and secondly, we do not think we do not think we know too much about just which items to put in that category. I think probably most of the people here are familiar with one of Professor Von Neumann's theories. I think it reduces to about this: we should not publish the census report; we should just keep it on tape and when you want to know what the number of children of school age in your community is, you dial some proper combination on your telephone, and our machine reads it back to you. But this is a long-range view.

J. M. Bennett (Ferranti, Ltd., England): What is the size of your regular maintenance staff?

J. L. McPherson: I refer you to the gentleman on your right for this, rather the two gentlemen on your right.

S. N. Alexander (National Bureau of Standards): Because the Census machine is presently being maintained under contract by the Eckert-Mauchly Company, I think that figure should come from them. I would like to say that the Census has four people in training to take over this task, and I believe it is far from enough, but it is a difficult field in which to recruit these days, as those of you who are trying to get electronic engineers know. I will turn the question over to Mr. Weiner. He can give the number of men he applies to this job.

J. R. Weiner: (Eckert-Mauchly Computer Corporation): We have a rather large UNIVAC group. The people in that group work both on test and maintenance of the machines. It is not the sort of thing you can give a direct answer to and say, three, four, or ten. The point is we put as many people on as are required at any one time. We may have two technicians and one engineer on it at one time. We may have three or four engineers on it at another time. But in general I would say that it runs perhaps two technicians and an engineer on maintenance periods, and on the emergency engineering calls, one engineer comes in to handle it. If it turns out that it is beyond his capabilities, he gets in touch with another engineer who also comes in. But I do not know of any emergency calls that have occurred that two engineers have been unable to handle.

Now, as I mentioned before, it would be very nice to have the engineers on duty full time and when the machine does break down the engineer is there to fix it immediately. It is really a question of how long you want to take to fix the machine. It is a rather complicated device, and if you have one man there and he is not familiar with the entire machine—if something goes wrong on Uniservo, for example, he is going to get in touch with the man who knows the Uniservos inside and out to come in and help him. Does that answer your question?

J. M. Bennett: Yes. It has raised another one, though. Do you propose to continue maintenance when you go to Washington, for example, with these technicians under training?

J. R. Weiner: The people under training are engineers, and we hope that the Census Bureau will be able to maintain the machine with the people that are undergoing training. I think Dr. Alexander may have something to say on that also.

S. N. Alexander: We are trying very hard to see if we cannot get an arrangement whereby the Federal agency owning the equipment provides the day and night nurses and we hope that the Company will provide the physicians on call, so that when it looks like the patient is in a bad way we can get expert attention locally. This should not be too difficult because in the Washington area if everything goes well, there will be three such machines within another year, and this certainly will justify some backstopping by the supplier of skilled people capable of helping out.

I think there is a point to be emphasized here. This machine is really two kinds of machines in contrast to the ordinary computing machine. It has such an unusual input system that the special equipment associated with the input system and the mechanical auxiliaries require one kind of specialization and the internal electronics require another kind of specialization. While it is perfectly possible for a man to be reasonably familiar with everything, I think to do really good emergency servicing you will need specialists.

I would also like to add to this information that the electronics side of the machine behaves remarkably well in comparison to the mechanical and magnetic devices judging from the maintenance reports which come to us as the holder of the maintenance contract. It is in that area where the greatest development is needed, and incidentally where we are putting the greatest pressure on the Company, with respect to the delivery of UNIVACS 2 and 3. I think it is

fair to say that there has been a response to this pressure. I expect to see Number 2 UNIVAC pass a more stringent acceptance test on the communication between the UNIVAC and the tapes.

J. Belzer (Battelle Institute): Mr. McPherson, I would like to know whether this equipment will at any time be available outside of the Census Bureau, or will the load of the Census Bureau still be great enough to keep it going, or perhaps do you feel you will need another UNIVAC?

J. L. McPherson: We certainly feel we have enough UNIVACS right now. We think that eventually we will have no trouble keeping three or four busy when we are in the relatively low phases of the 10-year cycle of census work. This I cannot document with statistics, however. We do not want another UNIVAC tomorrow certainly, because we are still learning how to make this one sit up and bark, and until we feel we know a good deal more about the one we have we will not be too anxious to get another.

We do have peaks and valleys in our use of the equipment. For example, as of right now the UNIVAC is short of work because we have had a rather unhappy two weeks most recently with the card-to-tape equipment. What the card-to-tape equipment has been turning out has been not acceptable; consequently, there is nothing for the UNIVAC to do. If somebody happens to have a nice, big, important problem in his back pocket and it is all programmed, and he said to me this afternoon, "Will you do it," maybe I could do it for him. By tomorrow afternoon this golden opportunity may be gone.

E. C. Carlson (Mutual Life Insurance Company): Can you tell me just how much equipment, tabulating or otherwise, you are replacing with the UNIVAC?

J. L. McPherson: I think I have to just say no, I cannot. I am afraid I cannot elaborate much on that. The Census has a tremendous installation of tabulating equipment, and UNIVAC has taken a big load off that equipment, but we have a tremendous census, too, so that we did not cancel out any equipment. We have plenty of work for the UNIVAC and all the other equipment that we have.

It might be interesting and amusing and enlightening to sit down and try to estimate just how much different equipment we would use to do jobs that we plan to do with UNIVAC. The fact is that on the one hand, those of us who know UNIVAC, have been too busy just trying to make UNIVAC work, and those of us who know the other equipment have been too busy making that equipment work.

B. V. Bowden (Ferranti, Ltd., England): Are you going to use the same equipment for the census of production as well as the census of population? Are you going to use the same equipment for doing other censuses, such as the census of production, the census of distribution, and the census of the retail trade and that kind of thing as well as the census of population?

J. L. McPherson: We are in the process of trying to answer that question ourselves. My own answer is yes, I would like to think that we will have a complete large-scale electronic computer processing of the so-called economic census. However, this is by no means certain.

If I predict, I will guess that we will do part of it using punch card equipment and part of it using the UNIVAC.

In the long run, we think the censuses will be tabulated through the use of the electronic equipment. At the Census we do a tremendous amount of what we call current survey work, much of which is based on small samples, and it is my own opinion that never will punch card equipment be replaced by this kind of equipment for the processing of some of the smaller samples. But the censuses of population, agriculture, retail trade, and manufacturing will in time be processed on this kind of equipment. The next economic censuses are for the fiscal year ending in 1953, I believe, which means that we get into the processing of those some time in the summer of 1954.

We hope, by then, to have techniques worked out for using the UNIVAC for those censuses.

The Burroughs Laboratory Computer

G. G. HOBERG

IN EARLY 1950 the Research Division of the Burroughs Adding Machine Company developed a need for a computing installation of moderate size which would, among other objectives:

1. Serve as a proving ground for new ideas and devices.
2. Provide data on large-scale-computer reliability.
3. Offer a means for indoctrinating a large number of inexperienced people in the various phases of realizing and operating a digital computer.
4. Produce useful solutions of engineering problems associated with a research program.
5. Solve business problems in a manner which would simulate their handling by contemplated smaller and relatively special-purpose commercial machines.

At this time Burroughs had already developed a line of unit-packaged computer-type electronic pulse circuits to facilitate research and development work on computer components, circuits, and systems. Known as pulse-control units, these system building blocks were based on similar ones in use at Project Whirlwind at the Massachusetts Institute of Technology, where the idea for this type of equipment originated in 1947. Large-scale use of such units to simulate the control and storage portions of the Whirlwind I computer, when only its arithmetic element had been constructed, established the intriguing possibility of their exploitation in the synthesis of directly useful high-speed digital-computer systems.

ENGINEERING APPROACH

Although the already designed pulse-control units were thought to be somewhat too versatile and too bulky for use as mere low level logical components throughout a complete computer, they offered what seemed to be a very reasonable solution to the problem of obtaining a flexible computing installation economically and in a short time. In May 1950, a decision was made to design and construct a computer which was to utilize pulse-control units wherever feasible.

In addition to pulse-control units, components which were considered at its inception to be suitable for the Burroughs Laboratory Computer were standard teletype equipment and a magnetic drum. Both of these were purchased.

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Particularly important contributions to the realization of the Burroughs Laboratory Computer were made by Edward W. Veitch, who was responsible for the logical design, and whose intimate knowledge of the logic resulted in the 48-hour checkout of the machine; Harry Kenosian, who designed the standard pulse-control units; and Joseph Chedaker, who assisted in the over-all physical design and who supervised all installation and construction work.

Credit also is due to the many other members of the Research Division without whose efforts and co-operation this project could not have succeeded.

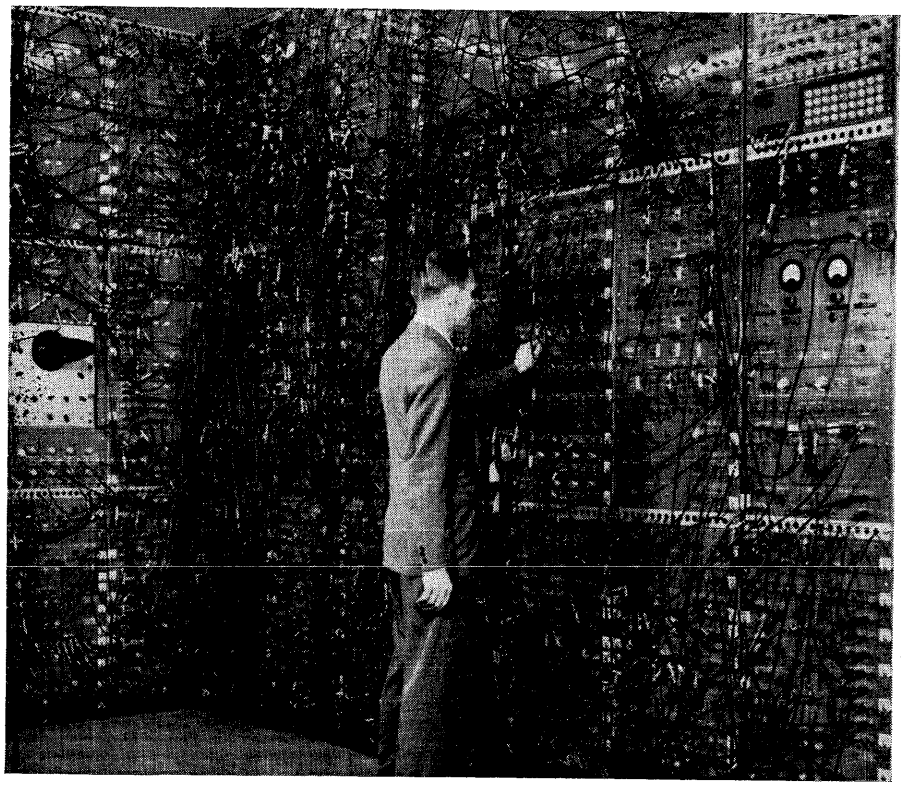

Figure 1. Right half of computer. Racks contain automatic and manual control systems

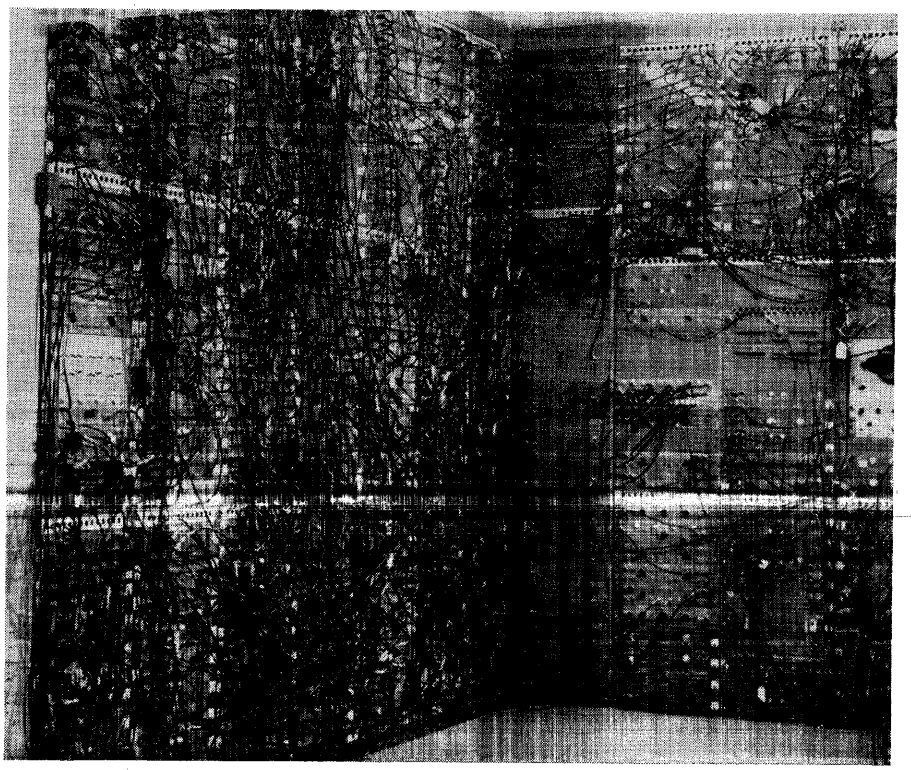

Figure 2. Left half of computer. Racks contain input-output control, manipulator, and portion of storage system

Engineering Research Associates of St. Paul, Minn., supplied the drum, together with much helpful advice and information on its use.

The availability of static magnetic registers of the type developed at the Harvard Computation Laboratory was not assured until a few months before completion of the computer. These registers, designed for another Burroughs project, offered the possibility of saving about 40 pulse-control units in the Laboratory Computer as then envisioned. The logical design was therefore changed to accommodate them. This adaptation, which did not at all affect the physical design of the computer, was the first concrete proof of the flexibility provided by the unitized approach.

Throughout the work of logical design, which represented the part-time effort of one individual, readily available equipment was the independent variable. Departures from this rule were made in only a few cases, such as that of a code-conversion function switch associated with the input-output equipment, where a minor custom-design task offered substantial opportunity to simplify the machine and to reduce its size.

Accomplishments

Despite occasional lulls in the effort caused by procurement difficulties and the pressure of other tasks, the Burroughs Laboratory Computer was completely operative in its initial form on February 19, 1951, just 9 months after the decision to design and build it. At this time it was turned over to programmers and logical designers for their indoctrination and use. After the mounting and interconnection of the units, the entire computer was completely checked out within 48 working hours, which time included that required to check and test the power system and its controls.

In light of the unusually short realization and checkout times, and the demonstrated adaptability of the machine to changes in logical design, misgivings about inordinate bulk and versatility in the units have been forgotten. Because all objectives were so readily achieved, the particular form of unitization employed proved to be an auspicious choice for the task at hand.

This computer is obviously not a neatly packaged commercial machine, (see Figures 1 and 2). Rather, it is a laboratory device which has been demonstrated to be a substantial asset to the research and development program of the Burroughs Adding Machine Company and should be evaluated on the basis of its performance in this role.

Systems Design

General Description

Although a number of changes have been made in the Laboratory Computer since its completion, the over-all arrangement of its principal component systems, indicated in Figure 3, has not changed. In all the variations which have existed up to this writing the computer has

been a general-purpose device capable of solving a wide variety of problems by appropriate programming. Changes in plug-in interconnections of the many building blocks are not required for each new problem solution.

As indicated in Figure 3, bulk storage of information is achieved by means of a magnetic drum. Standard teletype equipment provides input and output facilities. Static magnetic shift registers are used in the data-manipulating section of the machine. Except for transducer circuitry associated with these elements, almost all electronic portions of the computer are made up of pulse-control units.

Both the instructions and the data upon which the instructions operate enter the machine via the teletype equipment, usually from previously prepared punched paper tapes. Normally the instructions, which are modifiable by arithmetic processes, are stored on the drum before a computation begins and are executed one after another in a sequence which can be contingent upon previously calculated results. Operands are called forth either from the drum or directly from one of a number of tapes.

The current instruction repertoire is listed in Table I. Actual execution of most instructions requires less than 700 microseconds, but each access to the magnetic-drum memory may require up to about 17 milliseconds, the time for one drum revolution. Addition thus requires a maximum of 17 milliseconds. Multiplication and division require an average of 50 milliseconds.

Although the machine originally used only single-address instructions, a recent modification which was carried out in less than an hour provided for a programmable choice between 1- and 2-address operation, (see Two address, Table I). The 2-address system requires more storage space for the program, but with it careful programming can result in appreciably faster computation by reducing the effective average access time to the drum memory.

Table II shows the teletype-printer representation for the standard operand and instruction words used in the Laboratory Computer. Each decimal digit is represented in the computer by four binary digits in the excess-three code. Conversion between the standard 5-hole teletype code and the excess-three code is accomplished by means of crystal-rectifier function switches. The check digit, which can have only three values, is a modulo-three count of all binary digits having the value 1 in an entire word. Within the computer the check digit is combined with the sign digit to make one 4-binary-digit group, so that the standard computer word length is 40 binary digits.

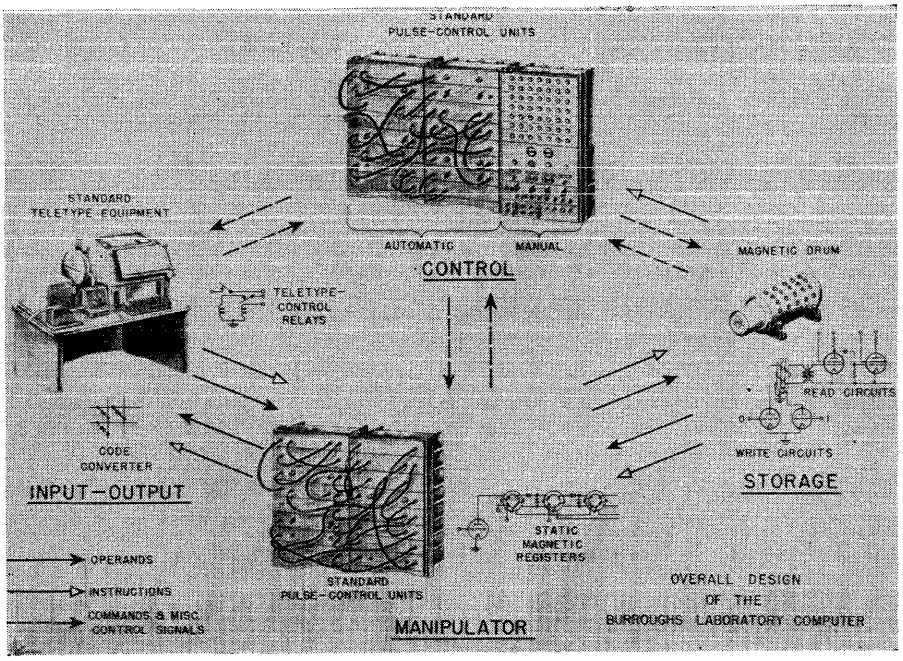

Figure 3. Over-all organization of computer systems

Input-Output System

In its initial form the input-output system consisted of standard teletype equipment (see Figure 4), which included a page printer, a keyboard, a tape transmitter-distributor, and an automatic reperforator. Operating speed of this standard equipment is about six characters per second. Although it provided all necessary functions, the original system was no paragon of speed, flexibility, or convenience.

Additional standard teletype equipment was therefore added to increase the terminal data-handling facilities of the machine. At this writing the teletype system is made up of the following standard units:

1. Two page printers, for recording both input and output data.
2. Two keyboards, with tape punches, for manual preparation of tapes.
3. Two reperforators, one typing, one non-typing, for automatic preparation of new tapes, especially from computer results.
4. Three transmitter-distributors for reading from tapes.

Units may be selected both manually and automatically.

The most recent enhancement of the terminal facilities is an experimental photoelectric punched-tape reader built for the Laboratory Computer on a

Table I. Laboratory Computer Instruction Repertoire

(November 1, 1951)

Address	Operation Code	
(x).....	(	....*Shift* (*SH*). Shift accumulator right x places
(m).....	/	....*Unconditional transfer* (*UT*). Obtain next instruction from first half of m
(m).....	!	....*Conditional transfer* (*CT*). Continue normally if accumulator contents are negative; otherwise, proceed as in UT
(x).....	0	....*Halt* (*H*). If x is 0 halt unconditionally. If x is 1 or 5, halt if appropriate switches are closed
(m).....	1	....*Add* (*AD*). Add contents of m to contents of accumulator
(m).....	2	....*Subtract* (*SU*). Subtract contents of m from contents of accumulator
(m).....	3	....*Read drum* (*RD*). Clear accumulator and insert contents of m
(m).....	4	....*Extract* (*EX*). Replace odd integers in accumulator with integers in corresponding digit positions of m
(m).....	5	....*Multiply* (*M*). Multiply contents of accumulator by contents of m
(m).....	6	....*Divide* (*D*). Divide contents of m by contents of accumulator
(x).....	7	....*Tape* (*T*). Perform input or output operation designated by (x)
(m).....	8	....*Photoread* (*PR*). Read from photoelectric reader into m, m+1, ... until tape marker or end of channel
(m).....	9	....*Write Drum* (*WD*). Write contents of the accumulator in m
(m).....	Sp	....*C-A interchange* (*CA*). Interchange contents of C register and accumulator
(m).....	-	....*Two address* (*2A*). Change operation mode from one-address to two-addresses or vice versa; obtain next instruction from m
(x).....	)	....*Switch band* (*SB*). Switch to band x of storage system

Table II. Laboratory Computer Word Structure

(November 1, 1951)

Operands:

012345678 3
674352643 – 1
- Check digit
- Sign digit (space plus, hyphen minus)
- Most significant digit

Instructions:

One-address

6437/5124 3
- Check digit
- Operation code, instr. (b)
- Operand address, instr. (b)
- Operation code, instr. (a)
- Operand address, instr. (a)

Two-address

6438/663x 2
- Check digit
- Address of next instruction
- Operation code
- Operand address

co-operative basis by several of Burroughs development projects from available techniques and breadboard equipment. Reading speed is about 100 characters per second. This device is intended primarily for bulk loading of the internal memory.

Storage System

The principal component of the internal memory is an Engineering Research Associates magnetic drum whose revolution time is about 17 milliseconds. Provisions for up to 218 magnetic heads mounted so as to give 16 tracks to the axial inch make the potential storage capacity about 440,000 binary digits. The pulse density used is 80 per inch.

In addition to a conventional timing track which provides 128-kc pulses for synchronizing purposes, two other control tracks are used:

1. The word-index track, which contains 50 pulses for denoting the starting points of the 50 words on each data track.
2. The address code track, which contains 50 7-pulse code groups for identifying the word-index pulses during the address-selection process whereby only a selected word is recorded on or read from a previously selected track.

Decimal digits are stored on data tracks with their component binary digits in time sequence. The decimal digits of each word are interlaced with those of another word to increase the time between them so that information from the drum can be sent directly into the lower-speed magnetic shift registers in the manipulator.

When the computer was first completed equipment for only six data tracks was available. Although this capacity was adequate for initial experimentation, it was soon increased to the planned sixteen tracks, that is, 800 10-digit words. In October 1951, 90 additional data tracks were added. The 106 data tracks available at this writing represent a storage capacity of 5,300 words, or a total of 212,000 binary digits.

Manipulator System

All arithmetic processes are carried out in the manipulator system. Initially, this system consisted of a single 1-word static magnetic memory, together with flip-flops, gates, and delays in the form of pulse-control units. Three such 1-word magnetic-memory units and many additional pulse-control units are in use at this writing. With the addition of the two extra magnetic-memory units, facilities for performing multiplication and division as built-in operations also were provided. These operations previously had been programmed in terms of more basic instructions.

Each of the three magnetic-memory units comprises four independent Harvard-type shift registers, each of which has capacity for eight binary digits. A unit is operated so that the four binary digits of one decimal digit are in identical positions in different shift registers, and so may be shifted into or out of the memory simultaneously. The circulating loop is closed externally by means of four pulse-control-unit flip-flops which provide the necessary ninth information digit. The combination sign-check digit associated with each word is handled separately.

For logical purposes the three magnetic-memory units, each containing four magnetic registers, are defined respectively as the *A* register (accumulator), *B* register, and *C* register. Because the data interlacing used on the drum results in 64 microseconds between successive shifts, about 16 kc is the maximum rate at which these registers are shifted. The pulse-control units, however, are operated at intervals as small as about 2 microseconds, because use is made of a total of three sets of timing pulses derived from the drum timing track by means of different external delays.

All arithmetic operations are essentially performed in the decimal system. The position of the decimal point is determined by manual switch settings. Decimal digits are added one at a time in true binary form by four binary adders. A built-in correction compensates for use of the excess-three code. Multiplication is done by over-and-over addition, and division by over-and-over subtraction. Addition uses only the *A* register, but multiplication and division require *B* and *C* registers as well.

Control System

As indicated in Figure 3, the control system can be broken down into automatic and manual portions. Both consist almost entirely of standard pulse-control units.

Automatic control consists of a number

Figure 4. Operators making step-by-step check of teletype input-ouput facilities

of counters, registers, and local control systems which keep account of all information required for carrying out the various instructions of a program and the low-level commands within individual instructions. The techniques used are generally similar to those employed in other large-scale electronic digital computers.

Almost everything which can be done by the computer under the supervision of automatic control can be caused to happen in a step-by-step manner under the direction of the toggle switches and push buttons of the manual control system. Where the formally established manual controls prove inadequate, access to the individual pulse-control units of the automatic control and manipulator system can almost always be made to yield desired results. An important part of the manual-control system is the bank of indicator lights which repeat, in an ordered array, the information represented by the indicators on all the widely separated flip-flops in the machine.

Engineering Features

General Description

The over-all view of the Laboratory Computer presented in Figures 1 and 2 indicates that physically the machine resembles a huge plugboard. Most of the equipment is mounted in 19 relay racks which stand in rows along three walls of a room at a distance of about 4 feet from those walls. Each 10-foot rack can accommodate more than 30 pulse-control units. Ventilation is accomplished by exhausting the air from the U-shaped volume between the racks and walls, the latter being provided with filtered air ports. Almost all of the tubes in the machine are located within the ventilated region.

At this writing, the machine contains a total of about 3,700 vacuum tubes and 7,500 germanium-crystal rectifiers. Approximately 2,500 plug-in coaxial cables interconnect 800-odd discrete units. D-c dissipation is about 12 kw. Total demand from the a-c lines is about 35 kva.

Except for an oscilloscope used for test purposes, only two kinds of equipment are mounted in the racks:

1. Standard pulse-control units;
2. Custom-designed units intended solely for use in the Laboratory Computer, some of which, namely, the static magnetic memory units, serve a second purpose by demonstrating the operational feasibility of techniques under consideration for use in other Burroughs projects.

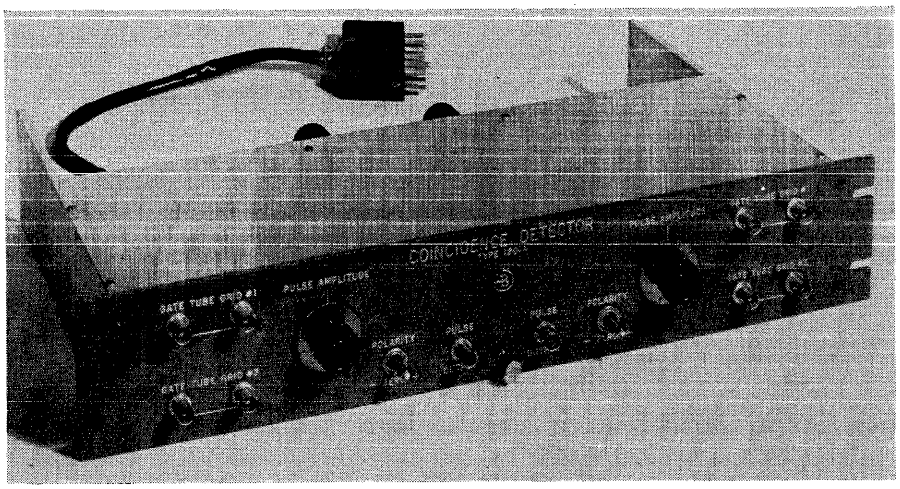

Figure 5. Typical pulse-control unit

Most of the 30-odd custom-designed units of about 15 different types are physically similar to the standard units. They account for fewer than 200 tubes, or about 5 per cent of the total tube count.

Four types of equipment are not mounted in the main racks:

1. The magnetic drum, which is located in the enclosure behind the racks, together with two small racks of auxiliary electronic equipment.
2. The standard teletype equipment, which is aligned along one wall of the room, adjacent to one row of racks.
3. The photoelectric punched-paper-tape reader, which is mounted on its own dolly.
4. Power transformers and the d-c power supplies, which are located in another room. The four identical general-purpose d-c supplies are in conformity with the over-all philosophy of unitization. They contain about 7 per cent of the total number of tubes in the machine.

Because the object was to realize only a laboratory device, and not a handsome and compact marketable machine, size and appearance were considered of little importance. Economy, convenience, and salvagability were stressed.

Pulse-Control Units

Pulse-control units contain electronic pulse circuits, for computer and similar applications, which are packaged at the flip-flop and gate level. Designed primarily for use in test setups which normally require only a half dozen or so units, the present line is satisfactory, but not optimum, for large-system applications.

A typical unit is shown in Figure 5. Pulse-control units are different from the plug-in units containing one or two vacuum tubes which are in widespread use at present because they contain both input and output buffer amplifiers, which make possible a high degree of interconnection flexibility. Signal connections are made by means of the jacks on the front panel. Power connections are made by means of the power cable and connector with which each unit is equipped.

Only two kinds of signals are transmitted between units on the plug-in coaxial cables:

1. Standard pulses, each shaped roughly like a half-cycle of a sine wave, with baseline duration equal to 0.1 microsecond.
2. Two-valued control voltages supplied by flip-flop circuits whose switching time is about 0.2 microsecond.

Most units will operate at a pulse-repetition frequency of 2 megacycles.

Output impedance levels are low and input impedances high, so that one unit can drive many others. The load limit on a unit providing a control-voltage output is determined only by the required switching time. Each 2-foot length of unterminated output cable and each driven input terminal adds about 0.06 microsecond to the switching time. A flip-flop unit connected to five vacuum tube coincidence-detector inputs by means of 23 feet of coaxial cable gives an effective switching time of of approximately 1 microsecond.

Unlike control-voltage cables, pulse lines are terminated in their characteristic resistance by means of plug-in resistors. The 0.1-microsecond pulses are therefore not much affected by the length of cable driven. Eight driven units represent the usual working maximum load on pulse lines. Standardization of signals and incorporation of buffer amplifiers establishes independence of one pulse-control unit from another in three important categories:

1. *Logical.* Each unit is a logical entity which corresponds to a discrete box in the usual lowest-level block diagram.

Table III. Pulse-Control Units in the Laboratory Computer

(November 1, 1951)

Unit Type	Function	Tubes per Unit	Units	Total Tubes
Flip-flop, type 1101A	Control, storage, counting	7	160	1,120
Coincidence detector, type 1201A	Pulse gating	6	281*	1,686
Coincidence detector, type 1202A	D-c gating	0	54*	0
Pulse delay, type 1301B	Unprecise delays, 1 to 80,000 microseconds	8	19	152
Pulse delay, type 1302A	Precise delays, 0.1 to 1.9 microseconds	5	14	70
Channel selector, type 1401A	Pulse distribution, manual control	7	18	126
Mixers, type 1601, 2A	Pulse mixing	0	200	0
Other units of six types	Counting, push button pulsing, relay switching, etc.		39	106
Totals			785	3,260

* Each unit contains two independent channels.

2. *Electronic.* Each unit is an electronic entity which can be connected to others without concern over electronic problems.

3. *Physical.* Each unit is a physical entity whose position in an array of equipment is substantially independent of the location of the source and destination of its signals.

Table III lists the types of pulse-control units and the number of each presently used in the computer, together with their salient logical features. These 785 units contain a total of 3,260 tubes, about 88 per cent of the total number in the computer. Note that some units contain no tubes, but only gating and mixing circuits comprising germanium-crystal rectifiers. These units are exceptions to the general rule in that they must be proximate to those which they feed, and are especially designed for this purpose.

Reliability

Table IV presents the performance record of the Laboratory Computer. No particular effort has been expended to achieve impressive reliability figures. The totals shown began accumulating within a few days after final assembly of the machine.

Tube trouble was the cause of about 95 per cent of the large amount of down time, 145 hours, associated with pulse-control units. After 1,500 hours only 77 per cent of the 1,000 *6AG7* pentodes and only 80 per cent of the 500 *6AN5* beam-power amplifiers from the original installation had survived. The *6AG7*'s have suffered from cathode peeling, and are being replaced by the manufacturer as an admittedly defective lot of tubes. Difficulty with the *6AN5*'s has been cathode-current instability which is greatly aggravated if heater voltages drop only a few tenths below normal.

A flip-flop design which allows the plate potential to be lower than that of the screen grid is believed to contribute to the *6AN5* trouble, although no ratings are exceeded. Close co-operation with the manufacturer is being maintained in an effort to solve the problem. More recent pulse-control unit flip-flops use *6AG7*'s with good results. The *6AN5*'s perform well in pulse circuits and JAN d-c tests.

Experience with other tube types has been satisfactory on the whole. Gradual application and removal of heater voltage over 5-minute periods is believed largely responsible for the fact that no heater failures have occurred since the initial checkout of the machine. None of the tubes installed originally were preburned, but because facilities have become available most tubes to be used in the future will have been preburned.

Only five germanium-crystal rectifiers of about 7,500 in use are known to have failed.

Evaluation of Engineering Approach

Advantages

Creation of a substantial portion of the Laboratory Computer by merely mounting and interconnecting standard pulse-control units resulted in the following variety of significant advantages:

Flexibility. Changes in logical design have been readily effected. New major systems components have been intergrated easily into the machine and others can be, provided they come equipped with necessary transducer circuitry.

Salvagability. At least 80 per cent of the bulk of the machine, including power supplies, is completely salvagable in terms of equipment in great demand on a number of different Research Division projects.

Engineering. The engineering effort devoted to this project was substantially less than it would have been if any other design approach had been taken.

Logical Design. Logical design was conducted in parallel with, rather than previous to, electronic design and construction. Final details were not available until about 1 month before the computer was completed. Not the least advantage in this category was the fact that the logical design did not require thorough checking as is customary when it is relatively irrevocable. The few logical errors which were inevitable were uncovered and corrected during the short checkout period of the machine.

Drafting. In contrast with the very heavy drafting load usually associated with the design and construction of a machine of comparable size, this computer was built from negligibly few drawings, except for those on the individual unit types.

Production. The usual advantages accruing to the synthesis of a large equipment from small identical units applied here. Most of the construction was carried out with little regard for the logical design, since the only logical data necessary were estimates of units requirements.

Trouble Location. The easy replaceability of units is not the only major asset of the pulse-control units during fault-tracing periods. The on-off pulse switches and the pulse amplitude controls are very useful tools, but perhaps the greatest advantage is the ability of the trouble shooter to remove signal cables and note the effects either of just removing them, or of plugging them into spare units usually available for test

Table IV. Laboratory Computer Performance Record

(Feb. 19 to Nov. 1, 1951)

	Hours
Available Time	
Operating time	1,102:42
Down time due to faults in	
Pulse-control units	145:20
Magnetic-drum equipment	16:13
Teletype equipment	23:16
Magnetic registers	11:16
Power system	24:23
Undetermined	3:49
Total down time	224:17
Total available time	1,326:59
% Efficiency $= \frac{\text{Operating time}}{\text{Available time}} \times 100\%$	
$= \frac{1,102}{1,326} \times 100\% = 83\%$	
Unavailable Time	
Engineering changes	202:28
Preventive maintenance	27:29
Total unavailable time	229:57

purposes. The level of manual access to the Laboratory Computer is such that an oscilloscope need rarely be used.

Training. Logical design personnel with little experience in electronics have been planning and carrying out physical changes in the machine with only technician assistance. Such experience is expected to have a valuable effect on the future output of these individuals.

Disadvantages

Following are listed some disadvantages attendant to the synthesis of the Laboratory Computor from pulse-control units:

Size. The machine is unquestionably bulkier than fundamentally necessary. Its tube count is of the order of 2.5 times greater than that which would be required in an efficient custom design for the same logic.

Appearance. See Figure 1. Some objections have been voiced to the appearance of a disordered array of cables on the fronts of the units, although the definition of front is a topic for discussion. These objections could be met by building a false front on the machine, but the matter has not been of sufficient importance to justify such expenditure of effort.

Reliability. The use of a greater number of tubes and other components than are basically required means that the fault probability is higher than the best possible figure. Also, since plug-in connections are inherently less reliable than soldered connections, the machine is more susceptible on this score than it would need to be. These facts have not yet resulted in appreciable difficulty.

Power. Dissipation is greater than necessary in the optimum custom design for two reasons:

1. The tube count is greater.

2. The circuits are all suitable for very high-speed operation, with consequent more lavish use of power than if they had only the required pass band in each individual case. A single high-speed flip-flop unit can dissipate as much as 50 watts.

Convenience. Because the units used in the computer had already been designed with only test-equipment applications in mind, removal and interchange of units is not quite so convenient as it might have been. On these units the cable connections are on the same side as that on which the units must be withdrawn from their mounting racks. A more recent mechanical design, which is a still unproved candidate for future use, is such that the unit is removable to the side opposite that occupied by the maze of cables.

Permanence. The ability to change connections readily no doubt will result occasionally in their being changed unnecessarily. Amplitude controls and switches present the likelihood of temporary changes being forgotten and leading to trouble.

One or all of these disadvantages might have been prohibitive in some applications, but collectively they have presented no undue difficulties in the present computer in its use as a laboratory device.

Applications

Because the principal reason for its existence is not the achievement of volumes of computed results, the Laboratory Computer has not been faced with a demanding problem-solving schedule. Emphasis has been placed on use of the machine for training, and as a means for checking the feasibility of new methods. It has been operated only during the normal 40-hour week.

The normal operating staff consists of three programmers and one maintenance technician. However, many other people in Burroughs' Research Division have had opportunities to become acquainted with the machine, both by setting up problem solutions and by participating in the engineering changes which have been carried out.

Despite the lack of pressure, a variety of problems have been solved. Most solutions have been for test purposes only, but some practical problems have led to useful results. The more significant practical problems dealt with to date are listed below.

Production Control. Sales forecasts and production parts lists were used to determine sample optimum production scheduling for Burroughs' Detroit plant. This effort will be renewed to utilize the recent improvements in terminal facilities.

Circuit Design. Required resistor and voltage values were computed for complex networks involving large numbers of crystal-rectifier gates and mixers. Results disclosed necessary design changes in a large computing system.

Logical Simulation. Tentative computer-system logical designs were expressed in equations from which the computer was able to simulate the logical performance of the device under design.

Cam Design. A practical engineering problem involving the design of a cam surface was successfully handled.

Miscellaneous problems which have been run for test and training purposes include matrix manipulations, random-number and prime-number generation, solution of linear simultaneous equations, and autocorrelation-function calculation.

The recent expansions of storage capacity and terminal facilities, and the incorporation of multiplication and division as built-in operations, have opened up new areas in which the Laboratory Computer can operate as an effective computing device. Its potential usefulness for handling business problems has been greatly increased. However, plans for the near future continue to emphasize the use of the machine as a laboratory device to an extent which will inhibit its accomplishments as a computing instrument.

Conclusions

The Research Division of the Burroughs Adding Machine Company has built a large-scale digital computer which is unique in that the internal mechanization of computational steps can be changed merely by reconnection of plug-in cables, see Figure 1. Construction from already designed general-purpose building blocks known as pulse-control units resulted in an unusually short time, only 9 months, between the decision to design the computer and its realization.

As implied by its name, the Laboratory Computer is a laboratory device whose most important function is to assist in a long-range development program of wide scope by providing a versatile proving ground for the trial and evaluation of new ideas and components. It is a useful source of engineering performance data, and has proved valuable as a means for training personnel.

Although problem solution has been regarded as a subsidiary objective, useful results have been obtained from the machine.

Initially its computational ability was modest, but recent enhancements have substantially increased its potential. These alterations have not yet been exploited to any great degree.

Basic limitations on its performance as a computer are the rotational speed of the magnetic drum, the only internal memory medium, and the speed of standard teletype terminal facilities. If further improved storage and terminal equipment becomes available it can

readily be added to the system, after first being equipped with necessary transducer circuitry.

Plans for the future continue to subjugate problem solution to use of the machine as a development tool.

Recommendations

Because the Laboratory Computer has fulfilled all of its objectives to a satisfactory degree, the building-block approach upon which its success is based appears worthy of consideration by others who have similar objectives or problems amenable to a similar design technique.

Although in all of its configurations to date the Laboratory Computer has been a programmable general-purpose computer, its engineering philosophy should be of particular interest to those who have need for smaller special-purpose and fixed-program machines, especially where the ability to change the logical design would be a substantial asset.

The method also is recommended where the need for a machine is only temporary, and where systems principles should be demonstrated before the engineering of a permanent machine is begun. Indeed, an aggregate of units used to establish logical feasibility might also serve as test and simulation equipment during the engineering design and final integration of a finished machine.

Discussion

W. P. Byrnes (Teletype Corporation): Did I hear you say that the information is put into the magnetic storage drum sequentially, binary digit by binary digit?

G. G. Hoberg: Yes, but it first goes into the arithmetic registers of the computer which serve as buffer storage. It is not put directly from the teletype equipment into the drum but rather from the teletype equipment into the manipulator registers and thence into the drum.

W. P. Byrnes: Is it put in the drum on a simultaneous basis?

G. G. Hoberg: No. These magnetic registers consist of four parallel magnetic shift registers, but the information is taken out of them only bit by bit: that is, all four registers are shifted simultaneously, so that one decimal digit and four binary digits come out of the register, into flip-flops. Then this information is picked up bit by bit and put into the drum at the proper time.

You see, it is fundamentally impossible here to read directly from teletype into the drum because they are both dynamic systems and it is difficult to synchronize them. You have to get information where it will be held for a while and then put it into the drum selectively at the proper time. This is done by the static magnetic register.

W. P. Byrnes: Your buffer registers, are they set up so they could accept the information from the teletype equipment on a simultaneous basis rather than a start-stop?

G. G. Hoberg: Yes. One word at a time is read from the teletype equipment normally, or there is at least a spacer between words. Digits are read essentially continuously, but in one word groups. All five binary digits are read from the teletype in parallel.

J. C. Simons (Westinghouse Electric Corporation): You have given us a good picture of what you have done. Would you give us a better indication of your plans for the future? Do you plan to use this machine for your own work on problems, for your own development, and more particularly do you plan to develop this into another machine, a package machine which would be available commercially?

G. G. Hoberg: There will be no direct development of this machine into another machine; that is, this is not the first model of some series of machines, the last of which is to be a commercial product. It is not like that. This is a general purpose computing installation whose function will not in the future be primarily the solution of problems. It will be used mostly as a versatile proving ground, where we can, if we get a new kind of magnetic shift register, integrate it into the machine, or if we get a new arithmetic unit, integrate it into the machine. We may try out some solutions of business problems which will be handled in the same way they will be handled in contemplated commercial machines, but this machine is unlike anything that Burroughs hopes to sell in the future.

The IBM Card-Programmed Electronic Calculator

JOHN W. SHELDON LISTON TATUM

TRACKING a guided missile on a test range now is the only way to make sure of its performance. At one Department of Defense facility this is done by planting batteries of cameras or phototheodolites along a 100-mile course. During its flight, the missile position is recorded by each camera at 100 frames per second, together with the camera training angles. Formerly these thousands of pictures from each of many cameras were turned over to a crew of computers, to determine just what happened. It took 2 weeks to make the calculations for a single flight. Now this is done on the International Business Machines (IBM) Card-Programmed Electronic Calculator in about 8 hours, and the tests can proceed.

Several dozen of the CPC's, as they are called, have been delivered and are already turning out answers as of the date of writing. This paper will then concern a field-tested and proved, mass-produced electronic calculator.

The forerunner of this machine appeared in the spring of 1946. It was the type *603* electronic calculator, the first mass-produced, commercially available digital electronic calculator. Input and output were on standard 80-column punched cards. This machine was followed two years later by the improved type *604* electronic calculator, like its predecessor designed primarily for commercial usage.

Engineers were quick to see, however, that these two machines were as powerful for technical as for commercial calculations. They offered the advantages of electronic computing speeds, rapid input and output via standard media, and availability; that is, they had already been delivered and were being maintained in proper operating condition. Their chief disadvantages were only a lack of memory capacity for larger problems and a lack of a line printing unit to permit immediate inspection of instructions and results.

These two facilities were first provided by an experimental combination of the older type *603* electronic calculator with a type *405* electric accounting machine. This proved to be so successful that the latest type *604* electronic calculating unit was combined with the latest type *402-417* electric accounting machine for printing and a proved electromechanical memory unit to form the Card-Programmed Electronic Calculator. Deliveries were begun in 1949, almost 3 years ago, and production is continuing at a steady rate.

The CPC has proved to be truly a general purpose machine. The following examples may serve to illustrate this point:

1. Neutron shielding calculations: determination of average penetration of neutrons into various types of materials. This important calculation was begun on the original *603-405* combination, and has been continued on the CPC.

2. Jet engine thermodynamic calculations: reaction parameters in a multicomponent system.

3. Production control calculations: determination of material requirements from so-called explosion calculations.

4. Helicopter vibration analysis: determination of the normal modes and frequencies of vertical oscillations and coupled side bending and torsional oscillations of helicopter fuselages.

5. Data reduction calculations of a wide variety of types.

The Card-Programmed Electronic Calculator, hereinafter called the "CPC," achieves its great flexibility and high output in a number of ways. Chief among these is the design of the arithmetic unit, which is also the logical place to begin a description of the machine.

The Arithmetic Unit

Pluggable Control Panel

The heart of the CPC is the type *604* arithmetic unit, shown in Figure 1. This is an electronic unit of approximately 1,400 tubes containing electronic storage units, an electronic accumulator of 13 positions, and electronic timing and control circuits which will control the operation of the unit at an operating frequency of 50,000 pulses per second. The fundamental electronic operations provided are addition, subtraction, multiplication, and division, which may be used singly or in any combination under control of a wired program established by the user of the machine.

The extreme flexibility of the arithmetic unit itself arises from the use of a pluggable control panel; that is, a control panel for which all connections can easily be made by hand. This makes it possible to have one control panel wired for floating decimal operations, with factors carried as significant figures times a power of ten; one for fixed decimal operations; one for special functions such as trigonometric and logarithmic; one for matrix inversion; one for selfchecking, for example, by casting out 99's; et cetera. Often a considerable saving in time for a specific purpose can be obtained by wiring a control panel specially tailored for the problem. These control panels are separate units inserted into the calculator, so they may be interchanged readily. Effectively, they tell the arithmetic unit what to do at electronic speeds with the factors it has received at electromechanical speeds. In other words, operation of the arithmetic unit may be thought of as taking place in two phases:

1. Reading factors and instructions to and from the electromechanical units of the calculator, at electromechanical speeds.

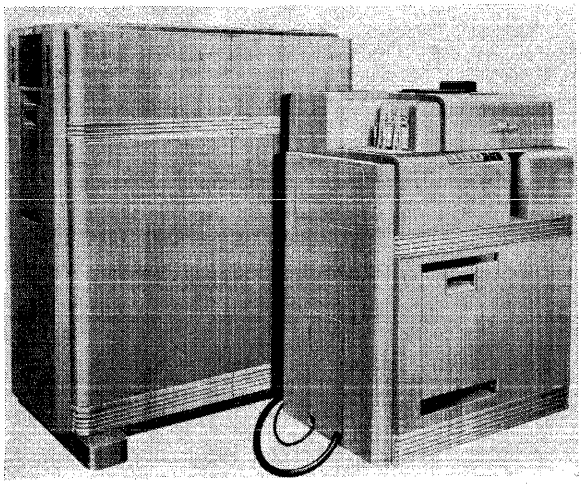

Figure 1. Arithmetic unit

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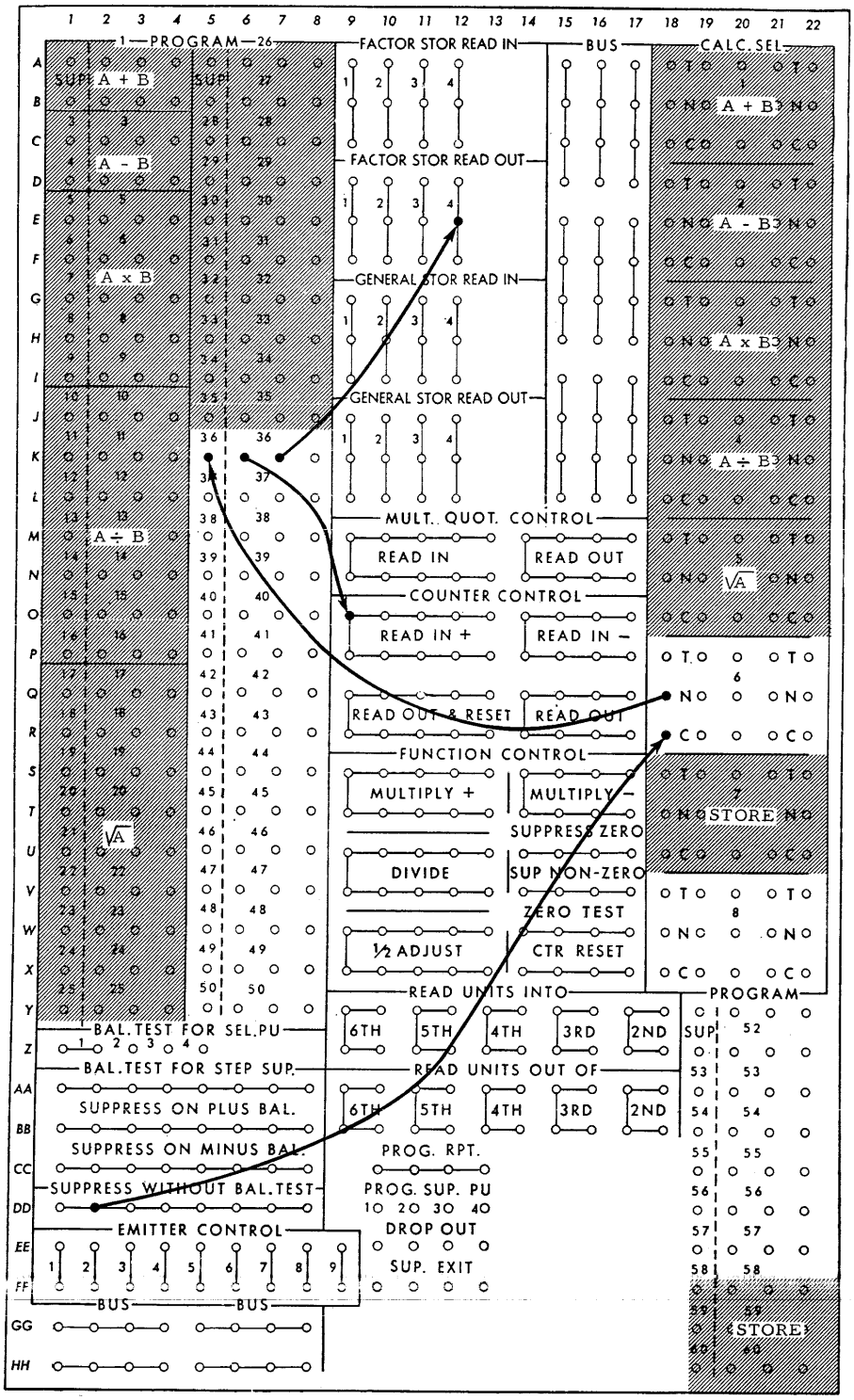


Figure 2. Control panel layout

2. Executing 60 program steps one or more times at electronic speeds.

Figure 2 shows the layout of the control panel, built up by plugging the necessary wires into the connection holes. On it 60 single-address commands or program steps are provided for manipulating the factors read into the arithmetic unit. To carry these out there is an electronic counter of 13 decimal positions and 37 positions of electronic memory, all interconnected by an 8-digit channel system.

A typical command may then be, "add the contents of electronic storage unit number 4 into the counter." This is illustrated in Figure 2 for program step number 36.

The following commands are available:

Storage read in
Storage read out
Multiplier quotient unit read in
Multiplier quotient unit read out
Counter read in plus
Counter read in minus
Counter read out
Counter read out and reset
Multiply plus
Multiply minus
Divide
One-half adjust
Zero test for step suppression
Column shift
Sign test for step suppression
Group suppress
Program repeat

Zero test, sign test, and group suppress enable designated groups of program steps to be suppressed selectively. These commands are specified by inserting a properly wired control panel into the machine. Various combinations of them may be selected by means of relays picked up by the operation instruction in each line of instruction. These relays are called calculate selectors, abbreviated calc. sel. on the wiring diagram. The wiring shown passing through calculate selector number 6 will make program step 36 active with an operation 6 instruction.

The wiring diagram, still Figure 2, shows how groups of steps are associated with calculate selectors to form operations in a general purpose 8-digit control panel. Thus it is possible for a single general-purpose control panel to offer a choice of the following: add, subtract, multiply, divide, sin x, cos x, hyperbolic sine, hyperbolic cosine, exponential, logarithmic, or square root functions, and other functions.

Ten by ten multiplication is performed by a partial products expansion. Ten by ten division is done by a quotient expansion. The calculation of special functions such as sin x and square root is effected by series expansions or iteration formulas.

The program repeat feature of the machine enables one to carry out these series or formulas at electronic speeds. This provides for a repetition, at electronic speeds, of all 60 program steps if specified conditions are not met. For example, if an approximate value generated for the square root does not agree closely enough with the previous approximation, the iteration will be carried out again.

A control panel utilizing all 60 program steps can be wired from a planning chart in 2 hours. Having a pluggable interchangeable arithmetic control panel best enables the user to tailor his own machine to his own problem.

Storage Units and Their Interconnections

The directing center of the arithmetic unit, which is itself of course the calculating center of the CPC, is the pluggable

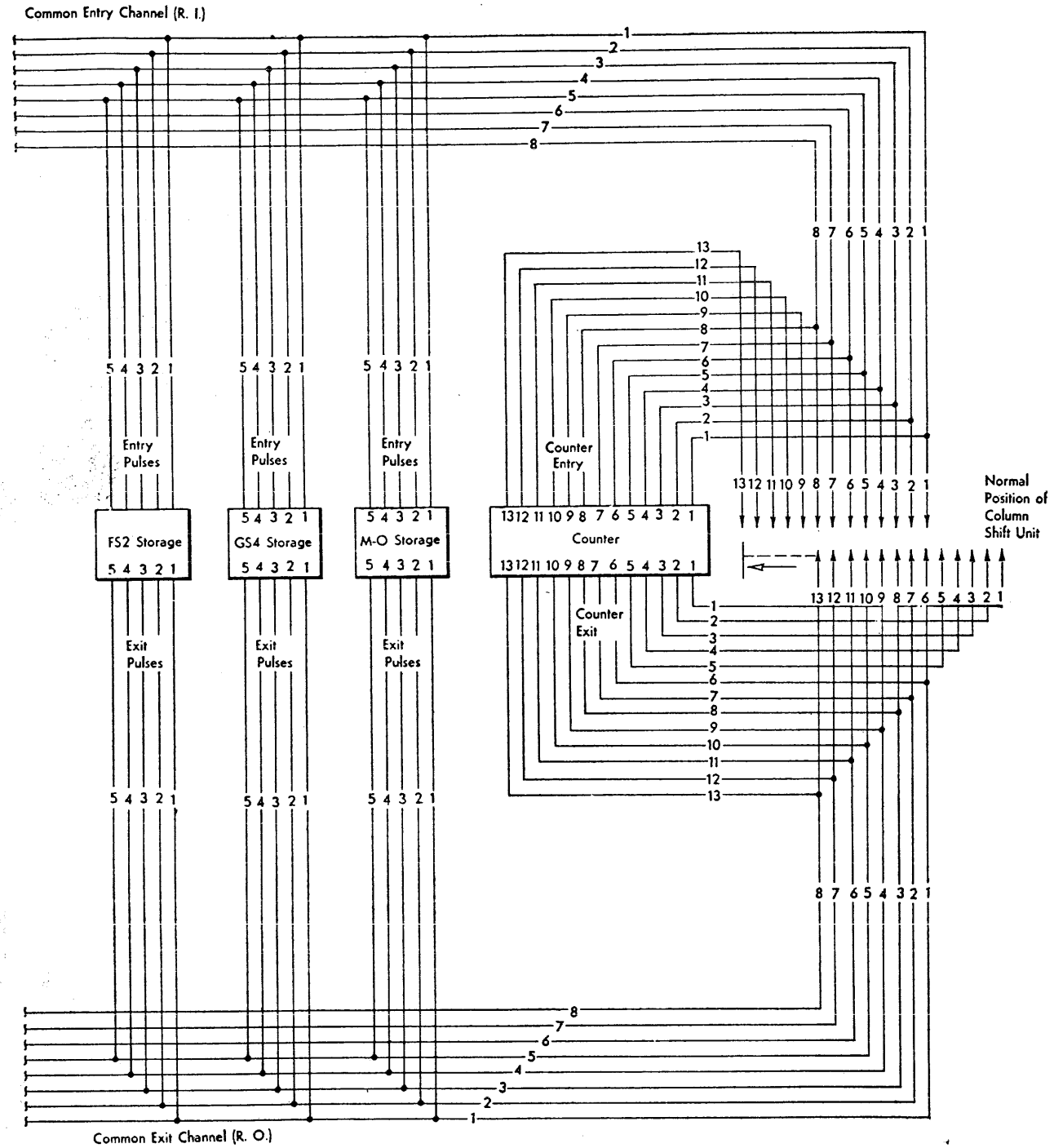


Figure 3. Interconnections between storage units

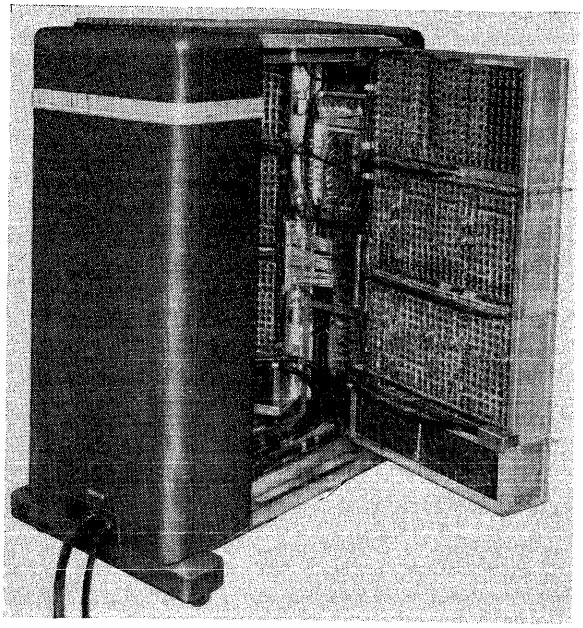
control panel, already described. The commands and operations specified by wiring on this panel are carried out by the various storage units, the counter unit, and their interconnections.

The arithmetic unit contains nine separate storage units with a total capacity for 37 digits and 9 algebraic signs. There is a 13-position electronic counter where additions and subtractions of algebraic numbers may be performed. Multiplication and division are performed by repeated addition and subtraction.

Figure 3 shows the interconnections between two typical storage units, the multiplier quotient (MQ) unit, and the counter. There is an eight digit channel for entry and exit from the storage and multiplier quotient units. These units may be connected into the channel in various ways by wiring on the control panels. The so-called normal assignment is the one shown. Information leaving a storage unit passes to the column shift unit where a shift left of zero to five digits may be effected before the information enters the counter or another storage unit. The column shift unit is controlled by the tertiary timer, to be discussed later, during multiplication and division and by control panel wiring during other operations. Information leaving the counter also passes into the shift unit, with the shift homed on the high positions of the counter, that is, position 6 of the counter connected to the units position of the channel. Thus a shift of from zero to five digits right may be effected. In this way the same shift unit serves for both right and left shifting.

Timing

The pluggable control panel and, to some extent, the interconnections between storage units serve to make



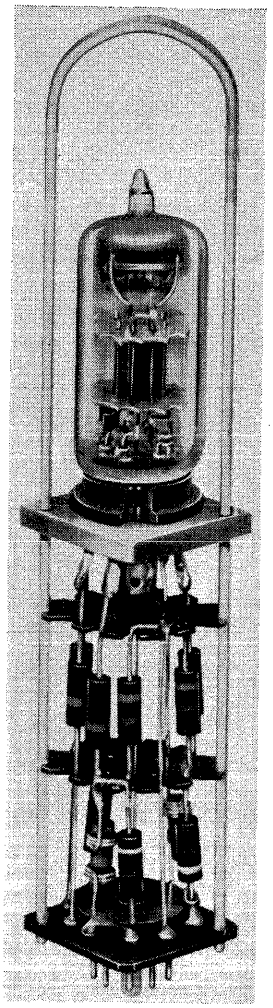
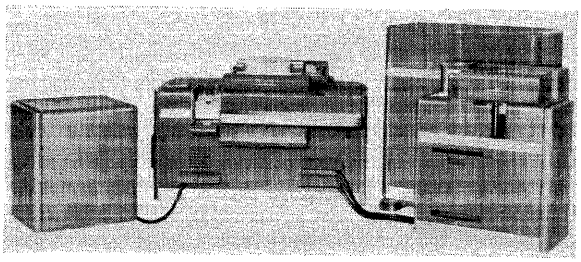


Figure 4 (above). Arithmetic unit, left gate open

Figure 5 (right). Pluggable circuit unit

Figure 6 (below). The CPC



the arithmetic unit of the CPC extremely flexible. At the same time it is recognized that certain functions of this unit not only do not need to be changed, but should be completely automatic, requiring no attention from the programmer.

Among these functions is that of timing, carried out by internal circuits as described in the following text.

Timing during calculation is governed by three timing circuits constructed from flip-flops. These are: the program control timer, the secondary timer, and the tertiary timer.

The program control timer steps the machine through the 60 program steps described above. Instructions are executed at each of these steps as specified by wiring on the control panel.

The secondary timer takes control each time the program control timer advances to a new step. It has 25 steps itself, which are executed at the fundamental frequency of the machine, 50 kc. This timer controls the actual execution of those orders which are wired on the control panel at the appropriate step in the program control timer. For example, if the number "5" is to be transferred into a certain storage unit, the secondary timer will control the reading of a pulse into the storage unit at one time, second pulse at two time, et cetera, up to a fifth pulse at five time, at which time the impulses will be cut off.

The tertiary timer controls the functions of the secondary timer during multiplication and division. It determines the number of times the multiplicand is to be added into the counter for each multiplier digit, when a shift should take place, et cetera. Since the calculator operates at a fundamental frequency of 50 kc, and since there are 25 steps in the secondary timer, one program step not involving multiplication or division takes 0.5 millisecond. This time includes that for all switching, column shifting, resetting, and adding. This is the fundamental time for addition, subtraction, and logical operations. The average time for multiplication (5 by 8) is 12.5 milliseconds; for division it is 16.3 milliseconds. These also are over-all times.

Special Features of Construction and Servicing

Much attention has been given in calculator design to matters of flexibility, control, and execution such as those previously described. If the resulting machine is to offer the greatest economy and utility, however, it is equally important that it be carefully designed for ease of construction and maintenance. This has been achieved in the arithmetic unit of the CPC through the use of gates mounting detachable rows of circuit components, and through pluggable circuit units.

Figure 4 shows a rear view of the arithmetic unit with the left gate open as for servicing. The program steps are located in the detachable rows of panel 2. Storage units are similarly located in panels 4 and 6. Panels 1, 3, and 5 in the right gate contain the secondary timer, tertiary timer, counter, and other special circuits.

Figure 5 shows one of the pluggable circuit units used in the arithmetic unit. The resistors and condensers in the circuit associated with a given tube are mounted in the assembly with that tube. Connections are made with the row chassis by means of a 9-prong plug. These pluggable units facilitate mass production. They also facilitate maintenance because the IBM customer engineer can trace difficulties by functional failure and easily replace the entire unit.

Over-all Operation of the CPC

Thus far the arthmetic unit, the heart of the CPC, has been described. As an independent unit, it is fully capable of handling problems requiring no more than 50 digits of machine capacity at a time, with limited sequencing. Indeed, provision is made for disconnecting it from the other units for separate operation. This leaves the electric accounting machine and the auxiliary memory unit free for work on an entirely different problem if desired.

For many problems, however, additional memory and sequencing capacity is desirable. For more complicated problems, it is almost essential to have a printing unit as well to record the results for immediate inspection. All these functions are provided by the connection of additional units to the arithmetic unit as shown in Figure 6, to form the complete Card-Programmed Electronic Calculator. From left to right these units are the type *941* auxiliary memory unit (two more could be attached), the

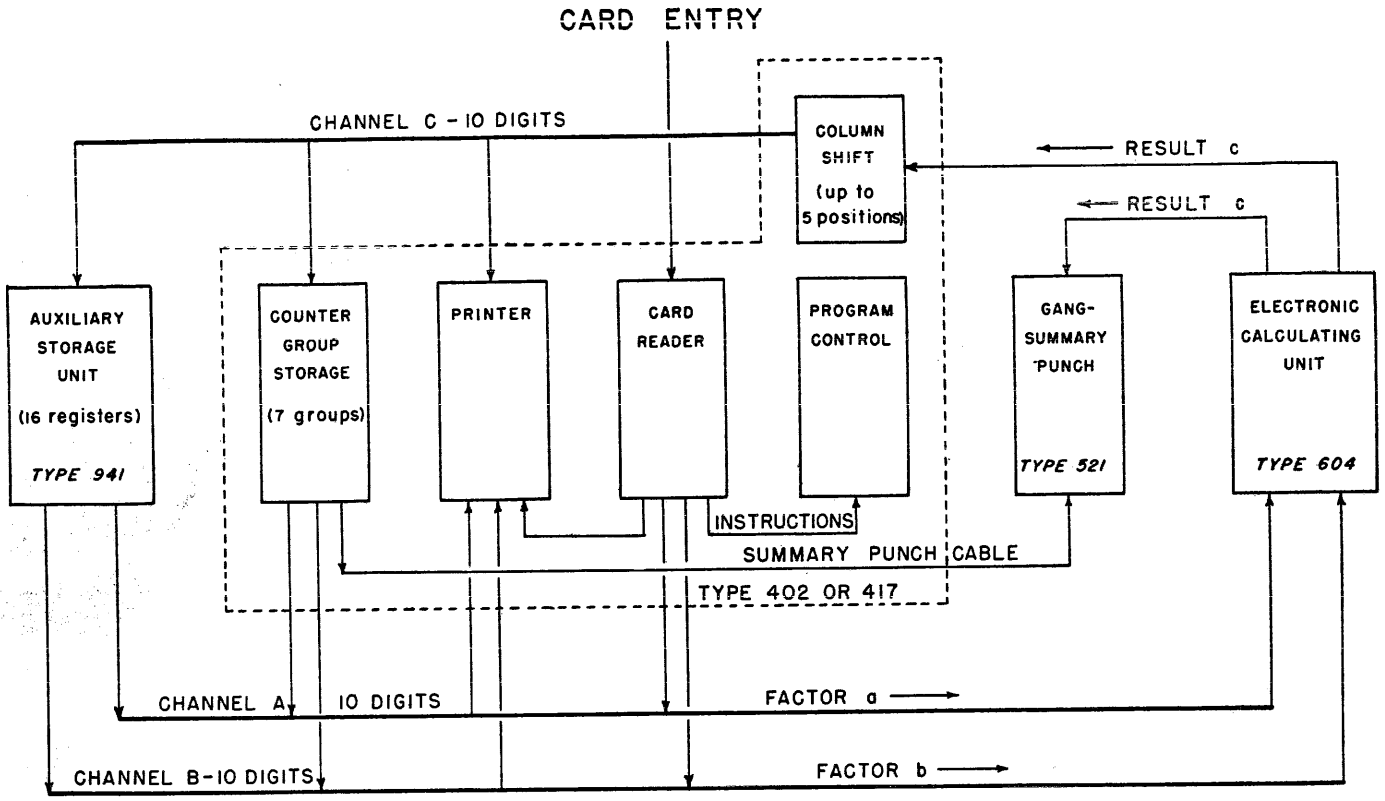


Figure 7. Connections between units by function

type *402-417* electric accounting machine, and the tube and the card-handling units of the type *604* arithmetic unit.

Figure 7 shows the connections between these units arranged by function. The electronic calculating unit at the right has already been described as the center of the CPC. The counter group storage, the line printer, the card reader, the column-shift unit, and the program control are located physically in the type *402-417* electric accounting machine. Normal operation is with numbers of ten decimal digits and algebraic sign. There are 80 counter positions in the counter group storage. Each type *941* auxiliary memory unit has a capacity for 16 such numbers, and up to three type *941*'s may be provided, for a total auxiliary memory of 480 digits plus 48 signs.

Both the electric accounting machine and the auxiliary memory unit operate by means of relays, cams, counter wheels, et cetera, and may be classified as electromechanical devices. The fundamental cycle for the operation of these units is 400 milliseconds. Thus there are two basic periods for operation in the CPC, namely, 400 milliseconds when dealing with the electromechanical units of the calculator, and 0.5 millisecond when dealing with the electronic component.

Clearly it is the object of the programmer to load up the electronic unit with as much information as possible, so as to minimize the number of electromechanical cycles. For problems which do not involve the calculation of special functions, the average time per operation can often be reduced to 150 milliseconds. When the program repeat feature of the arithmetic unit is being used to calculate special functions, the average time per operation may become as low as 10 milliseconds.

The electromechanical units are connected to the type *604* electronic calculator (arithmetic unit) by three channels, each carrying 10-decimal-digit numbers with sign (see Figure 7). The first two of these, channels A and B, carry factors and instructions to the electronic unit. The third, channel C, brings information from the electronic unit. Thus a series of calculations is normally reduced to steps of the logical form: a (operation) b yields c, where a and b are any numbers (constants, data, and previous results) to be combined by a specified operation (arithmetic, trigonometric, exponential, or other), and c is the result of this combination. In other words, the CPC operates with a 3-address coding system, normally read from cards. Each line of instruction contains the following:

1. An address code to direct the calculator where to find the number a to be read over channel A.
2. A similar code for locating the number b.
3. An operation instruction, $0(a,b)$.
4. A column shift instruction directing the column shift unit to shift the result c a specified number of decimal places.
5. An address code to tell the calculator where to store the result c.

The CPC operates using standard IBM punched cards. These are an economical, reliable, and flexible medium for intermediate and long-time storage of information. Cards are easy to reorder and merge using standard IBM auxiliary equipment.

A typical instruction card is shown in Figure 8. Note that it provides a full line of instructions, together with room for the introduction of one or two factors, variables or constants, to be read into the machine from the card. This leaves machine memory free for current operations. In effect, the instruction deck and interfiled data cards serve as an extensive auxiliary memory.

With this brief description of the overall operation of the CPC, and having pointed out some of the advantages of the arithmetic unit, one may turn to some of the outstanding features of the CPC as a whole. We shall consider sequencing, choices, parallel operation, and output.

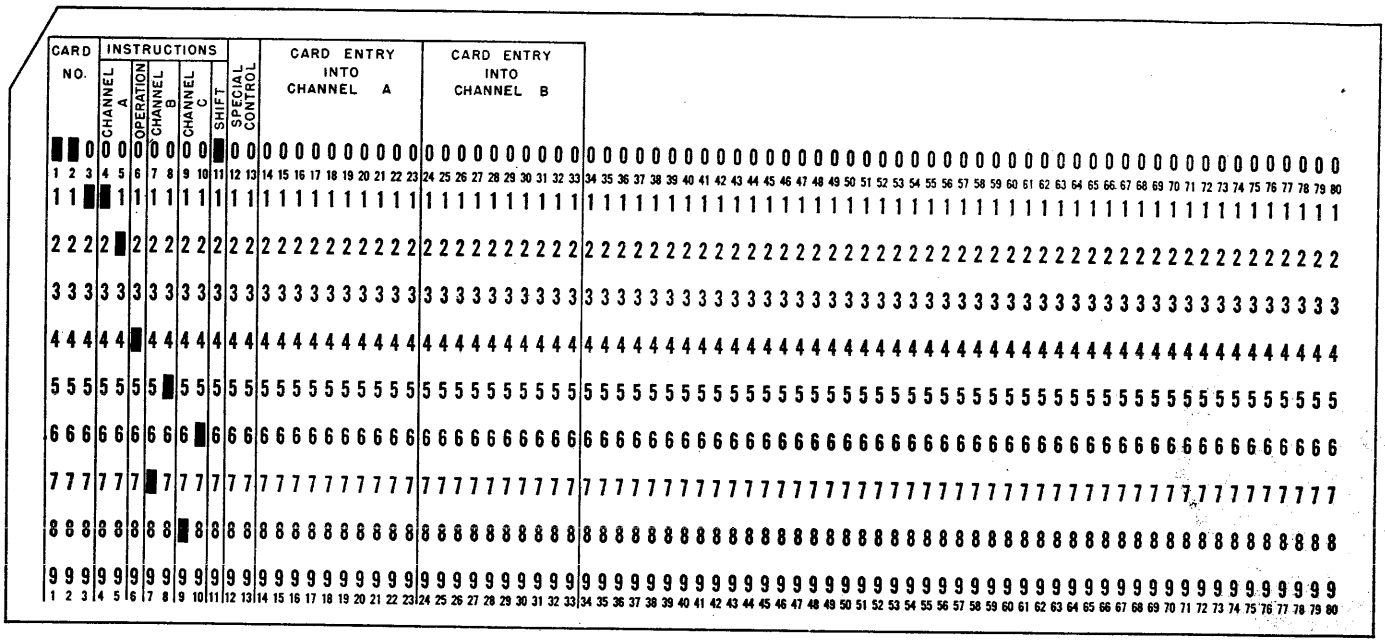


Figure 8. Instruction card

Sequencing

As the CPC usually reads its instructions from cards feeding through it, it is not necessary to allocate storage for program. Thus the CPC may be called an externally programmed machine. In an externally programmed machine there is no limit to the length of sequences which may be used. In a stored program machine, on the other hand, it is usually necessary to economize on the length of sequences, on account of the limited storage available. This usually makes it necessary to perform arithmetic operations on the address part of the stored instructions, in order to keep sequences short. Thus a stored program machine often has to keep reassuring itself as it goes along; that is, it has to keep asking itself questions. For example, in a direct matrix inversion the stored program machine has to keep asking itself such questions as: "Am I at the end of the row? Have I reached the last row? Should I go to the calculating sequence now?" In many problems the logical steps required to program a problem in a stored program machine may exceed by a factor of ten the actual useful arithmetic operations performed. External programming often gives the CPC a factor of ten in speed over a stored program machine with the same basic operation rate.

On the CPC one may choose alternate sequences from the instruction cards based on decisions made in the calculator. This is accomplished by picking up relays which alter the connections of the program control circuits to the reading brushes.

On the CPC subprogramming of up through ten lines of instructions may be effected by means of a relay network called a ten position field selector. Taking timed source pulses from a digit emitter, the field selector will emit up through ten lines of instruction in sequence.

This device is useful for calculating iteration loops, where a variable number of iterations may be required. The CPC can store instructions in memory when required.

Choices

When choices are necessary, they may be accomplished by wiring relay networks on the electric accounting machine control panel. For example, a number may have to be called from one of 16 different storage units, depending on a 4-binary-digit or 4-bit code. By using the 4-bit code to pick up four relays or selectors on the accounting machine control panel, this selection can be effected in one card cycle (400 milliseconds). To effect the same selection in a stored program machine might take many cycles.

Parallel Operation

While one operation is being performed in the arithmetic unit it is often possible to perform the additions involved in the problem in the electric accounting machine counters. Also, the choices described in the preceding paragraph take place without loss of time. All this is accomplished by pluggable relays or selectors together with normal instruction coding.

Output

The output from the CPC is in the form of punched cards and lines of printing. Output in cards is needed so as to have results available for future calculations and as intermediate storage in larger problems. Output of printed information is needed while the calculator is in operation for interpretation by mathematicians and for problem planning. On the CPC lines of instructions as well as data can be printed at a speed compatible with computing speeds. A line of printing consists of 89 characters and takes 400 milliseconds. Print time is simultaneous with other electromechanical functions of the machine, so that there is no time lost for printing.

This feature makes it easy to program problems for the CPC, and easy to deliver reports of results as calculations are completed.

Conclusions

The CPC demonstrates the advantages to be gained from constructing a large calculator of proved, mass-produced units; from utilizing a pluggable control panel for flexibility; from input and output via standard media; from external programming for an intermediate speed machine; from a measure of parallel operation; and from line-printing output operating simultaneously with computing.

A few of the applications for which the CPC has been used successfully are:

1. Systems of ordinary differential equations.
2. Systems of hyperbolic and parabolic

partial differential equations with two independent variables.

3. Elliptic partial differential equations with two independent variables.

4. Systems of linear equations.

5. Transcendental and algebraic equations.

6. Two-dimensional Monte Carlo problems.

7. Evaluation of multiple integrals.

8. Characteristic value problems.

A few of the areas in which the above types of problems have been solved are:

1. Wind tunnel and phototheodolite data reduction.

2. Aircraft and missile design and performance calculations.

3. Heat flow calculations.

4. Neutron shielding calculations.

5. Internal and external ballistics, including missile flight.

6. Chemical dynamics.

7. Engine design and performance calculations.

These applications are proof of the utility of the CPC as a design and research tool. The flexibility of the machine enables it to make a contribution in any field where calculating is required. Its speed and simplicity of programming make it well suited to the computing requirements of many diverse technical groups.

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Discussion

N. H. Taylor (MIT): Will the speaker make a few remarks concerning the percentage of time that the CPC operates, and then perhaps give an idea of the replacement rate of some of your tubes?

L. Tatum: May I say first that the production of these machines is the work of a very large number of people. For this reason we have asked representatives of other groups in our organization to give you more information on matters with which they are directly concerned. On this question I would like to introduce Mr. Dayger, from our Endicott Laboratories.

J. E. Dayger (IBM): I would say our experience today is that the "down time," including preventive maintenance, is running between 10 and 15 per cent.

I do not have the exact figures on tube replacement rate, but I will say that tube life has been a critical factor, particularly the *6J6*, which has been a major source of trouble. Other types of tubes have also given very poor life. However, there has been some experimentation with still other types which we believe will very materially improve our *6J6* units. A paper on IBM tube experience in detail will appear in the April, 1952 issue of *Electrical Engineering*.

W. P. Byrnes (Teletype Corporation): Can you tell us a little more about the input and output of the CPC? What is the speed of input?

L. Tatum: The input to the machine is in decimal form, read from a punched card. This card is fed into the "accounting machine" unit, where it forms an insulator between sets of 80 reading brushes and their brass rollers. When a brush passes through a hole in the card, it closes a circuit, giving an input pulse timed by the position of the hole. These cards go in at the rate of 9,000 an hour.

W. P. Byrnes: Is it 80 characters per line for the output?

L. Tatum: Eighty-nine characters per line at 9,000 lines per hour.

W. A. Ferrand (North American Aviation Company): Just what does the electromechanical memory consist of?

J. E. Dayger: The memory unit is the same electromechanical arrangement used in the *602-A* Calculator. It is like a mechanical counter. It operates in synchronism with the card feed and has a "stacked" readout. Each of the 16 units has a capacity of ten digits, plus sign.

F. M. Verzuh (MIT): You people have several general types of computers, the 602, 604, CPC, and your Selective Sequence machine. How have you determined which machines to use on different types of problems, and so on?

L. Tatum: Very generally I think that can be determined by the size of the problem and the speed with which an answer is required. In short, you don't send a boy to do a man's job. On the other hand, if you are watching dollars and cents, you don't send a man to do a boy's job, either. Usually we try to work with the people who are using our equipment, to help them determine themselves when they require a larger or faster machine. It is a problem of many angles, different each time.

L. A. Ohlinger (Northrop Aircraft Company): One of our men by the name of Reiss has developed a technique for using the CPC to program some of its own operations. A problem formerly requiring an instruction deck a yard high can now be done with a deck only 7 inches high. We are certainly satisfied with this, and will be glad to describe it for anyone who might be interested.

L. Tatum: We certainly would like to hear about it. We encourage the dissemination of information such as this.

The CPC has a 10-position 10-way "relay", by which it can be caused to emit its own programs up to and including ten lines of programming. Is that what you use?

L. A. Ohlinger: In combination with other things.

M. H. Kraus (Eckert-Mauchly Computer Corporation): I would like to ask more about components and reliability. Can you give us some ideas of the relative reliability of tubes and other parts of the computer? What about diodes?

J. E. Dayger: We do not use diodes to any extent. It is principally tubes and relays and circuit breakers that give trouble, and the main source of difficulty is still tubes.

R. E. Breisemeister (Consolidated Edison Company of New York, Inc.): Is it feasible to read information in from the punch unit? And, from the user's point of view, is it possible to call out the correct rate schedules from the auxiliary memory units?

L. Tatum: That depends on the size of your rate schedule. It is not only possible, it is being done on millions of bills every month, using the 604.

R. E. Breisemeister: We have a number of 604's, but our rate schedules are so complex that no more than two can be put into a single 60-program-step control panel. Under these conditions it is entirely impossible to do what you are saying.

L. Tatum: Are your rate tables more complex than an eight place table of logarithms? As mentioned in the talk, it is often possible to avoid the use of large tables altogether (such as a table of logarithms), and cut out that memory requirement simply by generating the function at electronic speeds.

G. T. Hunter (IBM): Let us return to the first of Mr. Breisemeister's questions, about reading from cards in the punch unit. At the present time, you cannot read from the punch unit into the calculator, basically because the punch unit and the accounting machine unit read the cards in opposite directions.

The second question concerned storing the rate tables. So far, utility companies have not been able to set up rates in even, geometric patterns. If that could be done, many of our accounting procedures would be simplified. But the present rate structures must be stored, either in a memory unit internally, or in the punched cards.

The ORDVAC

R. E. MEAGHER J. P. NASH

THE ORDVAC is a general purpose machine which has been built by the University of Illinois for the Ballistic Research Laboratories at Aberdeen, Maryland. The design has followed in a general way that of the computing machine discussed by Burks, Goldstine, and von Neumann in the "Preliminary Discussion of the Logical Design of an Electronic Computing Instrument" issued in 1946 by the Institute for Advanced Study.[1]

We are indebted to the Computer Project at the Institute for Advanced Study for much information and many suggestions such as the basic philosophy of an asynchronous machine with direct-coupled circuits. Furthermore some of the circuits in our machine are the same as those of that machine and some others are similar but differ in detail.

It is convenient to display the characteristics of the machine by means of Table I. Some of these will be described in more detail in the appropriate sections which follow. For this purpose we shall divide the machine into five parts: the arithmetic unit, the input-output, the memory, the control and the power supply. Two general views of the machine, with and without its covers, are shown in Figures 1 and 2.

Arithmetic Unit

The arithmetic unit is made up of three parts: the registers, the adder, and the digit resolver. The registers are four in number, the accumulator, the arithmetic register, the number register, and the order register. The register gates and flip-flops used in the ORDVAC follow exactly designs furnished by the Institute for Advanced Study. Of the registers named above, the latter two are nonshifting registers each of which consists of 40 binary digits held in 40 flip-flops. Information is communicated through them to the arithmetic unit and control from the memory. The number register holds addend, multiplicand, and divisor for arithmetic operations. The order register receives from the memory all orders to be handled by the control.

The shifting registers (accumulator and arithmetic register) each consist of two rows of 40 flip-flops, one row above the other. Since a nonshifting register contains one row of 40 flip-flops, two nonshifting registers can be made out of one shifting register, and the appearance of the ORDVAC is that of a machine with three double registers.

In addition to the two rows of flip-flops, a shifting register also has two rows of gate tubes. These gate tubes furnish four gates for each stage of the register—two "up" gates and two "down" gates. The "up" gates transfer straight up, while the "down" gates transfer down one place to the left or one place to the right. The bottom row of a shifting register holds the digits while they are being sensed during an operation; the top row is used as transient storage. A shift is accomplished by clearing the upper row, gating up to it from the lower row, clearing the lower row, and finally gating down either one place to the left or one place to the right. When shifts are made in this way information is not cleared from one location until it has been deposited in another.

Figure 3 illustrates part of a register, the down gates into a lower flip-flop being shown. The plate supplies of a flip-flop come from busses which are normally at +150 volts but which can be lowered for the purpose of clearing the flip-flop to either state. Thus if the supply to pin 1 is dropped, the flip-flop is put into the 1 state. The 1 state is arbitrarily defined as the state when pin 2 is high and is distinguished by a neon on pin 2.

The plate of a gate tube goes to the plate of the flip-flop to which information is being transferred; the gate grid is attached to the grid of the flip-flop from which information comes. When the gate cathode is lowered, the gate tube conducts if the grid is high and changes the second flip-flop if it is connected to the high plate.

This means that the second flip-flop must be in the proper state for receiving the gated information. Suppose a down right gate is wanted. First, F_3 is cleared to the 0 state by lowering pin 2, thus making pin 1 high. Then the cathode of G_R is lowered. If $F_1=0$, pin 6 is low, G_R does not conduct, and F_3 remains in the 0 state. It is thus the same as F_1. On the other hand, if $F_1=1$, pin 6 is high and G_R conducts. This causes pin 1 of F_3 to fall and turns F_3 to the 1 state. Therefore F_3 is the same as F_1.

The gating up in the registers is similar to the gating down except that only one "up" gate is ever used. This results in an extra set of gates which are not needed for shifting operations and are thus available for other use.

Access to the memory is in parallel from the accumulator and information from the input is supplied serially to the accumulator, utilizing the shifting properties of the register to put it in.

Similarly, the output is made serially from the arithmetic register, it being possible for the memory to communicate with this register.

The adder is a Kirchoff adder. It is basically the same as that in the Institute for Advanced Study machine, but it differs in detail, largely because of the difference in power supplies. The addend and augend digits control gates from two constant current sources which can allow current to flow through a summing resistor. The carry from the preceding stage controls the input voltage to the summing resistor. There are four possible voltages across the summing resistor, depending upon whether the sum at that particular stage is 0, 1, 2, or 3. If it is either of the latter two, a carry is produced for the next stage.

It may be seen in Figure 4 that the summing resistor is a 10,300-ohm resistor and the constant current sources are cathode followers supplying 4.85 milliamperes. The carry causes the input voltage to the 10,300-ohm resistor to

Table I. ORDVAC Characteristics

Machine type	Parallel, Asynchronous
Register capacity	40 binary digits
Memory capacity	1,024 words of 40 binary digits
Adder carry time	9½ microseconds
Allowed carry time	13 microseconds
Addition time	42 microseconds
Multiplication Time (all ones, positive multiplier)	1,000 microseconds
Multiplication time (all zeros, positive multiplier)	570 microseconds
Division time	1,000 microseconds
Memory period	24 microseconds
Time to load entire memory	38 minutes
Time to print contents of entire memory	38 minutes
Number of tubes	2,718
Machine d-c power	8.3 kw
Machine a-c power	8.8 kw
Total primary power (including power supplies and blowers)	35 kw
Kind of input	5-hole Teletype tape
Input system (space is 5 holes)	Sexadecimal
Output system	Sexadecimal Teletype
Number of digits assigned to an order	9
Number of digits assigned to memory address	10
Number of orders available	Greater than 50

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drop from 210 volts to 160 volts. The result is that the four voltages are in 50-volt steps, being 204, 154, 104, and 54 volts respectively. The time required to propagate a carry through the 40 stages of the adder is $9^1/_2$ microseconds.

The digit resolver is required to convert the adder voltages back to digital information. The addend and augend come into the adder from the accumulator and the number register, and the sum is returned to the accumulator after passing through the digit resolver. It is the function of the digit resolver to distinguish those sums having the digit 1 left in a stage from those having a zero. The former are the quantities 1 and 3 (having binary representation 01 and 11) while the latter are the quantities 0 and 2 (having binary representation 00 and 10). The digit resolver thus furnishes 0 volts for the accumulator if the adder output is 204 volts or 104 volts and furnishes −40 volts if the adder output is 154 volts or 54 volts.

Input-Output

The input-output equipment consists of modified Teletype units of the kind which were developed by the Bureau of Standards for the Institute for Advanced Study. It operates at standard Teletype speed, although the input has frequently been operated at about twice standard speed. The input is by means of standard 5-hole Teletype tape of which four holes are used to represent numbers in the sexadecimal or base-16 number system by means of a binary code. A 40-digit binary number is then written as a 10-digit sexadecimal number.

Output from the machine can be either to a tape punch or to a teletypewriter. In either case it is in the sexadecimal system, although if it is desired the output can be programmed and converted by means of a simple routine to decimal quantities.

The input and output are slow and in this facility the machine is unbalanced for some types of problems. At present consideration is being given to speeding both operatons up by a factor of about five, but beyond this no immediate increase in speed is contemplated.

Memory

The memory is of the electrostatic "Williams" type using 40 *3KP1* cathode-ray tubes.[2] Each cathode-ray tube stores 1,024 binary digits and can receive binary information from one digit of the accumulator and can release its stored information to the corresponding digit of the arithmetic, number, or order registers. Thus the total storage is 1,024 words of 40 binary digits. A slave cathode-ray tube and a 40-position switch are provided so that the contents of any one of the operating tubes can be viewed at one time. The cathode-ray tubes are operated with their deflection plates and second anodes at about 150 volts positive with respect to ground and with their cathodes at about 1,900 volts negative with respect to ground, giving an accelerating potential of about 2,050 volts.

Each cathode-ray tube is mounted in a horizontal position with its own shield consisting of a layer of copper, a layer of mu metal, and then a second layer of copper and a second layer of mu metal. Each cathode-ray tube is provided with an adjustment for intensity, focus, and astigmatism.

Associated with each memory tube is a chassis which can be seen in Figure 2 and which contains a 4-tube "video" amplifier with a gain of about 50,000 for a 1.5-microsecond pulse. The chassis also contains the logical circuit to provide for regeneration in the usual way and

Introductory Remarks

The following introductory remarks by **Dr. Herman Goldstein** *of the Institute for Advanced Study, preceded the presentation of this paper:*

Primarily, I wanted to say just a few words about the over-all history of the computer field with minor remarks about some of the things that characterize the machines that Dr. Meagher is going to discuss.

The history of the subject is extremely ancient. There has been and always will be a great need and desire not only in the obvious field, such as engineering, where answers are wanted for quite specific and quite clear reasons, but also in both pure and applied mathematics for results of an essentially computational nature. The desire to compute, then, is very old, but the mechanisms, as we well know, have been rather slow in development in any substantial way, and any of the things of the sort we are interested in can be traced to the confluence of two evolutionary streams in the last war. On the one hand, there was a development of electronic techniques in radar guidance and, on the other hand, an extremely pressing need among mathematicians for practical results. I think our present field of modern computation represents the confluence of these two evolutionary streams. But I would like to say a word about the particular thing which I think makes it possible.

Clearly, what one does in a computing machine is to represent mechanistically what a human computer performs. If it were not for the deep functions of the human intellect we would never be able to produce a machine. Fortunately, if one looks at what goes on when one does a computation, he finds it is possible to relate or resort to the ordinary vocabulary and transmit it to a computer in a dozen or so different words. Also there are problems of analysis characterized by this fact: that the total set of instructions in the "Pidgin English" of a dozen or so words, would run roughly to one printed page of instructions. One wants then to do this same page over and over again, perhaps each time changing some of the parameters which enter into the page. Therefore, it is possible to mechanize computational work and it is this fortunate fact, I think, which is the key to the whole success of the modern work from a logical level, at least.

Now, a word about the type of machines which Dr. Meagher is going to describe. It is true, there are a fair number either built or being built. All differ in certain respects but are of sufficient fundamental likeness that it is possible for me to say a word about them collectively, and for Dr. Meagher to essentially describe them all in describing the one at the University of Illinois.

The first thing about these machines I would like to mention is that they operate in a binary number system as distinguished from decimal machines. I do not particularly want to go in to processing methods and number bases, and of course the human does operate at base ten, but it is difficult to understand why there is any necessary reason for a mechanism to operate in the base ten. Therefore, one asks what is the best number of base to operate from? One thing that immediately strikes one—all machines have a logical and arithmetical part. The nature of mathematical logic is its binary character. So there is some reason for feeling the binary system has a certain advantage from that point of view. From the point of view of the arithmetic, the fact is that most of the units that one can produce electronically are fundamentally binary in character and to use another number base, such as base ten, one has to pyramid them. There is necessarily a certain wastefulness in such operation, because it takes four binary devices to produce a decimal digit. So one obtains, essentially, using groups of four binary devices, the ability to build up a decimal system. Since in this case it is possible to recognize 16 states and one uses only 10—six are lost. But I will not go into the subtleties that go into this machine. Suffice to say, it is binary. Secondarily, it is parallel, namely that all of the digits of two numbers are operated on simultaneously instead of starting seriatem with a pair and then a pair, et cetera.

The third classification is that these machines all use Williams' tubes; all use 40 of them in parallel, I believe. That is, all the deflection plates are swung in parallel with one digit for each of the 40 tubes. Some use 2-inch, some 3-inch, some 5-inch tubes.

I think this, by and large, describes the broad features of this type of machine.

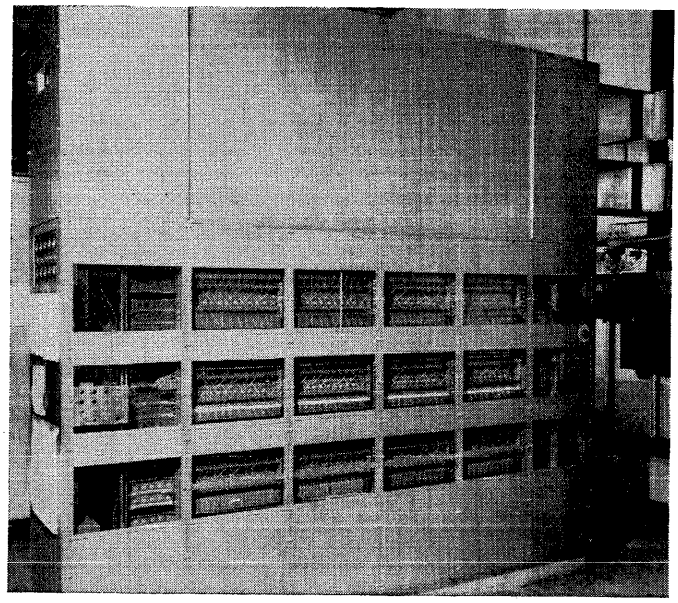


Figure 1. A front view of the ORDVAC showing the registers

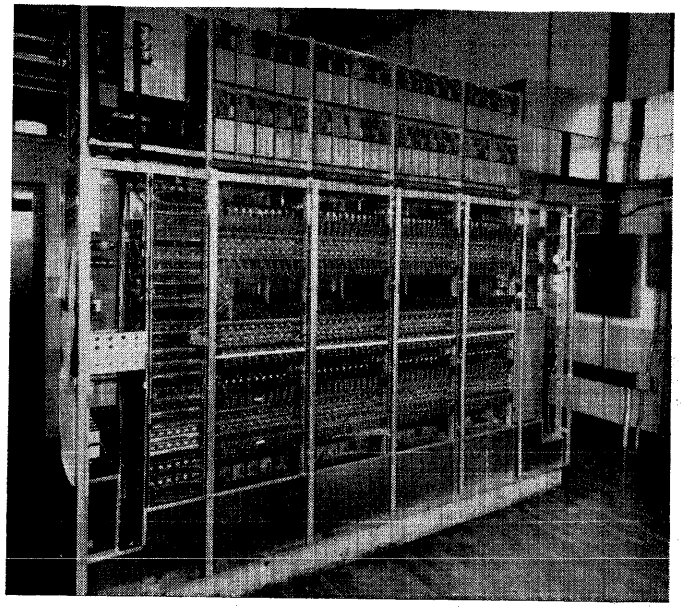


Figure 2. A front view of the ORDVAC without covers. The upper section contains the memory composed of 40 *3KP1* cathode-ray tubes and their associated chassis

for transfers of information to and from the appropriate registers. The output of this chassis is capacitively coupled and then d-c restored to the grid of the cathode-ray tube. The "2-dot" system of storage is used where the sensing position of the beam is called the dot and the other position is called the "dash." The beam is on for about 1.2 microseconds in the "dot" position and about 2.5 microseconds in the "dash" position. The period between cycles of memory operations has commonly been set at 24 microseconds, although all of the useful operations, including the clearing and gating of information, require about 16 microseconds.

The voltages for the deflection plates of the cathode-ray tubes which specify the position of the beam for each of the 1,024 memory addresses are obtained from an "address generator" which converts ten binary digits into 32 vertical positions and 32 horizontal positions by adding the currents from five binary stages for each. Some special care has been taken to insure that the deflection voltages are free from noise by providing special regulation for two of the voltages and by suitable limiting of the voltages on the wires which carry the ten binary digits to the "address generator."

It seems appropriate to summarize the useful performance of the memory with the following remarks.

It is necessary to check the adjustments of each memory tube daily by observing the video signals on an oscilloscope when the memory is in active use so that the signals corresponding to both dots and dashes can be seen. It is usually necessary to adjust about two or three intensities each time this is done.

We are currently using 40 *3KP1* tubes having a total of about 50 flaws on their phosphor screens which are bad enough to prevent satisfactory storage. About 15 of the 40 tubes have no flaws of this type. A process of tube selection is presently under way to reduce the flaws but the present 40 tubes represent the best 40 out of about 175 tubes. Currently we are operating by moving the raster on all 40 tubes in such a way that it does not use any of the flaw positions.

If one defines the "read-around-ratio" as the number of times that a dash can be read into or out of a single address without causing a nearby dot to change to a dash, and assuming that no regenerations occur, then it is possible to state that out of the 40,960 storage locations about three have a read-around-ratio as low as 20, about 20 have a read-around-ratio as low as 32 and about 200 have a read-around-ratio as low as 50. The way in which these results have been obtained is explained in a later section.

Control

As has been mentioned the control of the ORDVAC is direct coupled and asynchronous. Rather than have an external timing device for signalling each of the operations it is to perform, it operates by having each of its operations signal the one to follow. The speed with which it operates is therefore determined by its own ability to carry out the sequencing operations which are required. Since it is direct coupled the machine will simply stop if no signal is supplied for an operation. On the other hand, the machine can be made to stop by deliberately inhibiting a signal.

Let us consider one flip-flop F and two operations A and B as shown in Figure 5. When F is in the 0 state, A occurs and causes F to turn to 1. This initiates B which returns F to 0, and the sequence is repeated. Thus one flip-flop can be used to sequence a pair of operations. In the same way, n flip-flops can be used to sequence 2^n operations.

There are obvious defects in the simple example just cited. In the first place, the signal from A may turn F to 1 before A has had a chance to do its work. If this happens, the enabling signal to A will disappear and A will never be completed. Secondly, B may take place while A is still on. This could have disastrous results if the two signals were related, as, for example, when A clears a register and B gates information to that register. If B gates while A is still on and, worse still, if B never gets really turned on, the information would never be gated.

In order to prevent failures of these kinds, safety circuits have been designed into the ORDVAC control. These circuits do the following things:

1. They make the turnover requirements for control flip-flops more stringent than the turnover requirements for the flip-flops being controlled. Therefore, if the latter do not turn, neither will the former, and the machine will stop.

2. They require that when a control flip-flop is being turned over and sensed, the

signal from it be used only when it has been positively turned.

3. They require that before an operation in a sequence can occur the previous operation must not only have taken place but that it must also have been turned off.

Examples of circuits of these kinds may be found in the shift sequencing control. Shifting in the ORDVAC requires four operations, two clears and two gates, and these are sequenced with two flip-flops. Let us take a look at one of these flip-flops, the one which is turned over by a register gate bus. But first let us recall the register gating.

When the cathode of the gate tube is pulled down from +10 volts to −10 volts the contents of the second flip-flop will transfer if the grid was positive. Flip-flop grids are either 0 volts or negative about −20 volts. Since the cutoff of the *6J6* used for gating is about −4 volts, the gate will start to conduct when the cathode is at about +4 volts, and the transfer will have occurred by the time the cathode gets to 0 volts.

The same gate bus which pulled down the gate cathodes in the register is used to turn the control flip-flop F (Figure 6). But now the gate tube G is pegged at −5 volts instead of at 0 volts. This gives a 5-volt safety margin in the turnover of F, and it can be safely assumed that the register flip-flops turned over if F did.

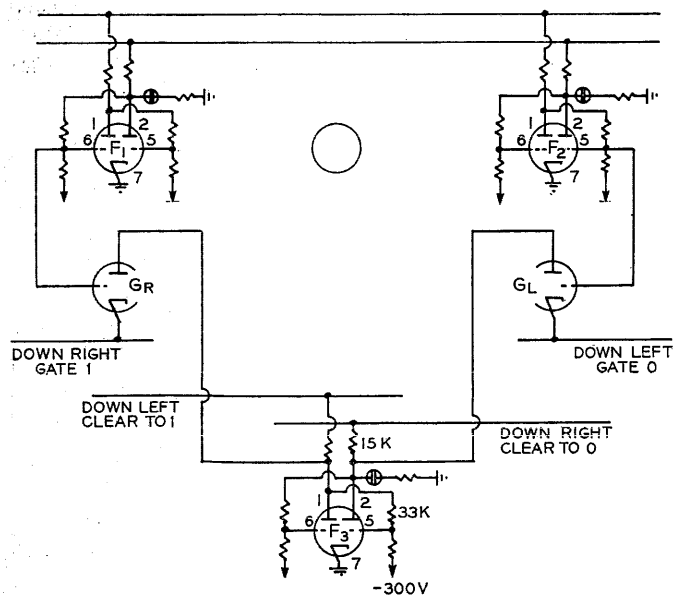
Negative signals are used in nearly all of the ORDVAC control. Before F was turned, pin 6 was negative. After it is turned by G, pin 5 is negative, and one might be tempted to take the signal for the next operation from here. But this would be a mistake, for pin 5 might go far enough negative to initiate the next operation before F is safely and permanently turned over. Therefore the signal will be taken from the positive-going grid 6 which is the last moving element of F. It will be sensed with the inverter N_1 which is built just like F. Because of the cutoff properties of N_1 it will not conduct until the grid gets up to −4 volts, and by then we know that F is safely over. The output of N_1 therefore says that the register gate bus has gone down and that F has been turned over. The turnover of F will shut off the gates in the register.

We still need to know that the gate bus is back up again before proceeding with the next step. This information is obtained from the inverter N_2. With pin 5 pegged at +5 volts, the signal from N_2 will not be negative until the gate bus is safely off again. The outputs of N_1 and N_2 then go to the "and" circuit A which starts the next operation when its cathode goes negative.

This is the kind of philosophy which has prevailed in the design of the control. Throughout the control an effort has been made to assure the safe operation of each step. If any step should fail, the result is not a loss of the information in the register but merely a "hanging up" of the machine. The control waits until the proper enabling signal comes along, and then it proceeds. This kind of construction makes it possible to test the operation step by step by putting switches in appropriate places so that the turnover of flip-flops can be controlled. One such place is in the cathode of the gate turning over the flip-flop F in the previous example. If this switch is open, the register gate will not turn off and the machine will wait until the switch is closed.

A price must be paid for these safety features, and the price, of course, is speed. The machine will run faster if it is not necessary to wait for checks on the operation. It will also run faster if operations are done as much as possible in parallel. Here again, although the ORDVAC is a parallel machine, a price has been paid in speed for convenience in doing certain control operations sequentially rather than in parallel.

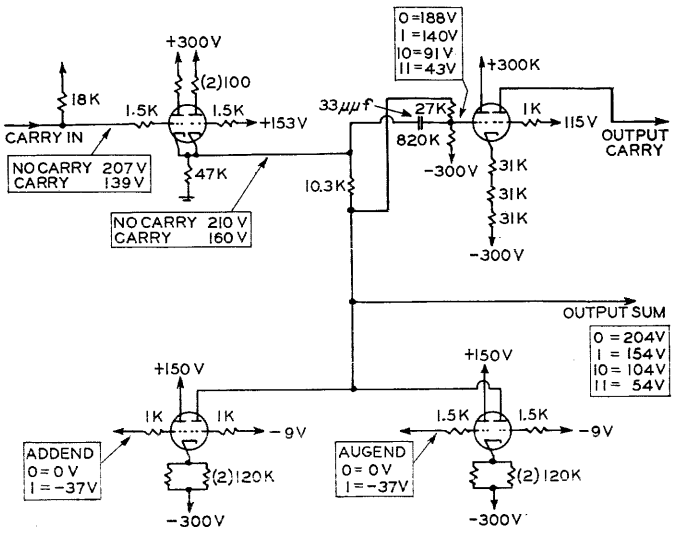
The ORDVAC memory is synchronous with a period of 24 microseconds. When the control is carrying out operations which do not involve the memory, it works independently while the memory regenerates its storage locations. But if an operation requires use of the memory, the control and memory must be synchronized for one 24-microsecond interval, called an action cycle. In order to get into synchronization the control furnishes a signal to the memory. Since this signal may occur at any time during the 24-microsecond cycle, the control must then wait for an appropriate memory pulse, the action sense pulse, to come along. When this pulse comes, the action cycle normally takes place. During this cycle information is transferred to or from the memory, the necessary clearing and gating operations for these transfers being executed more or less directly



FLIPFLOP STATE	PIN 1	PIN 2	PIN 5	PIN 6
0	HIGH	LOW	HIGH	LOW
1	LOW	HIGH	LOW	HIGH

Figure 3 (left). Register circuit showing two upper flip-flops, one lower flip-flop and the "down" gating system

Figure 4 (below). Analogue adder showing input for addend and augend, output, and the carry circuit



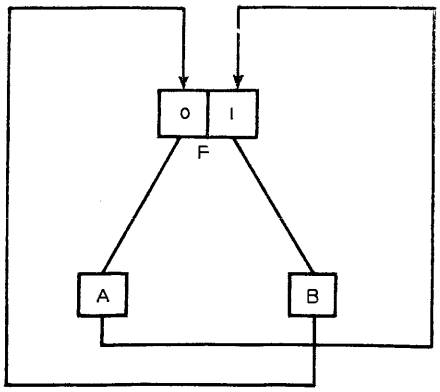


Figure 5. A single flip-flop F used to control two operations A and B in sequence

by the memory pulses themselves. This one case where the memory clears and gates in the registers is the only synchronous control operation in the machine.

The action cycle ends when the next action sense pulse occurs 24 microseconds after the one which began the cycle. At this time a "have used memory" signal goes to the control to indicate that the use of the memory has been completed. The memory returns to regenerating, and the control resumes its asynchronous activity.

The synchronization process requires two flip-flops. One distinguishes between an action cycle and a regeneration cycle. The second distinguishes between the time before the action cycle, when the memory is still regenerating, and the time afterward when it has returned to regenerating but while the "have used memory" signal is on.

A large part of the control is devoted to setting up the proper clear and gate sequences for the registers. Fundamentally, of course, everything that is done in the arithmetic unit must be a combination of sensing flip-flops, adding, clearing, and gating. The decisions about these things are made after certain combinations of digits, called orders, have been decoded with logical circuits. The number of orders that is actually necessary for the convenient coding of the kinds of problems which the ORDVAC is expected to solve is probably between 20 and 30, and this many orders can be described with 15 flip-flops, ten of them being needed for memory addresses. A decoding matrix using five flip-flops would then be used to cause one of 32 wires to be actuated whenever the corresponding order is presented. However (as suggested by the group at the Institute for Advanced Study) since there are 20 digits available for an order of which only ten are needed to describe the 1,024-memory locations, we can use as many as ten for an instruction. Actually nine have been used with the result that the number of tubes required for decoding has been decreased and the number of orders has been increased. The number of orders which has actually been used in programming is about 50, some of which were not forseen when the control was designed. A complete matrix is not used, the decoding circuits being made up of a number of submatrices.

The arithmetic of the machine is one which handles numbers in the range from -1 to $+1$ (actually excluding $+1$) and which carries negative numbers as complements relative to 2. This is the kind of arithmetic which was described by Burks, Goldstine, and von Neumann.[1] However, the methods described by them have not been followed in the arithmetic operations of this machine. In particular, the method by which multiplication is carried out is not used, as far as we know, in any other machine. (This method was suggested by Mr. J. E. Robertson of the University of Illinois.)

Multiplication without roundoff by two positive numbers poses no problems. If an operand x is negative, the machine holds the number $2+x$, and if the sign digit of x is ignored multiplication by a positive y gives the result $xy+y$

Figure 6. Safer way by which flip-flop F can control an operation A

(A) Block diagram (B) circuit

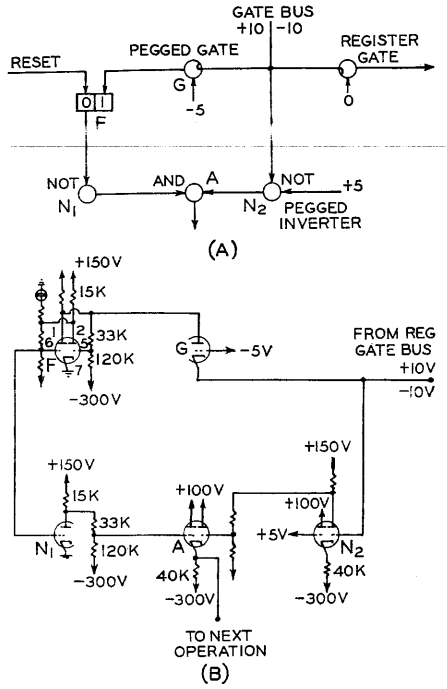


Table II. Multiplication with Negative Multiplicand Showing System Given in Burks, Goldstine, and von Neumann and System in ORDVAC

Multiplicand 1.101 Multiplier 0.101

Operation	Multiplier Digit	Accumulated Product
Burks, Goldstine, von Neumann		
(1) Add multiplicand without sign	1	.0.101
(2) Shift right		.0.0101
(3) Change sign and shift right	0	.0.10101
(4) Add multiplicand without sign	1	.1.01001
(5) Shift right		.0.101001
(6) Add correction term 1.001		.1.110001
ORDVAC		
(1) Add multiplicand	1	.1.101
(2) Divide by 2		.1.1101
(3) Divide by 2	0	.1.11101
(4) Add multiplicand	1	.1.10001
(5) Divide by 2		.1.110001

so that subtraction of y will give the desired answer. If x is the multiplier, there is no difficulty because y is available at the end and can be subtracted. But if x is the multiplicand, y is lost during the process of shifting to inspect its digits. Hence it must be subtracted during the stepwise formation of the partial products. The method proposed by Burks, Goldstine, and von Neumann which does this, requires varying the gating of digits to the adder as well as making a "correction" at the end.

The ORDVAC multiplication scheme makes no distinction between positive and negative multiplicands. This is accomplished by making an algebraically correct division by two at each step, and always adding the complete multiplicand with its sign if an addition is required. No corrections are required at the end. The same circuits are used as those which carry out the right shift order, this order giving a correct division by 2 in the accumulator. A sample problem may be followed in Table II.

The problem posed by the roundoff, which requires that the product be rounded to a sign and 39 places after the addition of 2^{-40}, has been solved by doing the roundoff before the multiplication begins. If there is no roundoff, the accumulator is cleared and the product xy is formed. If there is to be a roundoff, the accumulator is cleared, 2^{-1} is gated into it, and the quantity $xy+2^{-40}$ is formed. Since the accumulator holds only the sign and first 39 digits of the product, it holds the rounded product.

This method of rounding off has the advantage of being fast, because there is no need to do an additional step at the

end which involves waiting for carries in the adder, and it also provides the facility for gating the digit 2^{-1}, into the accumulator for other orders. In connection with a shift order a digit can be put any place in the accumulator without requiring additional memory storage space.

The division process is different from the nonrestoring process described by Burks, Goldstine, and von Neumann and is almost the inverse of the multiplication process.

Power Supplies

The machine uses about 8.8 kw of a-c power to operate the filaments of the vacuum tubes.

The d-c power consumption is:

−2,000 volts	0.09	ampere
− 300 volts	16.0	amperes
+ 100 volts	10.1	amperes
+ 150 volts	3.8	amperes
+ 300 volts	5.2	amperes
+ 680 volts	0.4	ampere

The −2,000-volt and the +680-volt potentials are obtained from vacuum tube regulated power supplies which were built at the University of Illinois.

The intermediate four voltages supply the bulk of the d-c power for the machine and insofar as possible all circuits have been designed to use these voltages directly without additional regulation or "bleeders." In a few cases such as adder circuits "odd" voltages are required and these are furnished by a "bleeder" which supplies voltages for vacuum tube grids where the current drain is very low. These four "main" voltages are furnished by commercially built and controlled rectifier units which are regulated against line voltage changes and fast and slow load changes to ±2 per cent.

All of the d-c loads are divided into separate circuits of about 3 amperes each and arranged with individual fuses in such a way that the failure of any individual circuit will open a relay thus turning off a "holding circuit" on all of the d-c power.

Operation of the ORDVAC

To date no mathematical problems other than trivial ones have been solved by the ORDVAC. A considerable number of test routines have been run, some of them having 100 words or more and using some 25 of the available orders of the machine. Most of the more complicated routines have been concerned with testing the memory for read-around-ratio, although they serve also, of course, to test the arithmetic unit and control at the same time.

One of the more useful routines is one which tests every storage location of the memory for its read-around characteristics. The raster now is arranged so that the spots form hexagons. The routine is put into the top of the memory and causes the first spot in the lower half to be bombarded a given number of times with dashes. It then inspects the surrounding spots, which have been previously cleared to dots, to see if any have become dashes. If so, it causes the tube number (0 to 39) and address of the bombarded spot to be printed. This is repeated for all of the addresses in the lower half of the memory. The routine then transfers itself to the lower half and inspects the upper half in the same way. At the end of the complete inspection it changes the number of bombardments and repeats the process.

A program for the over-all testing of the machine has been run. This program generates a set of 352 pseudo-random numbers b_i and stores them in successive memory locations. It then performs multiplication and divisions of b_i by b_{i+1}, checking multiplication results by multiplying in both directions and comparing and checking division results by multiplication. If all of these are correct, the numbers are transferred to 352 other locations and the transfers are checked. If there is no failure, i is increased by one and the process is repeated, transferring each b_i to a different address this time. When i reaches 352 (a major cycle), the process starts again.

At any failure the machine prints pertinent data and stops. Upon being started again it goes through a subroutine which checks all of the principal orders, trying to find the cause of the first failure. If an order fails, the machine again furnishes information and stops.

This program ran continuously for 12 hours and then failed when one memory location changed from a dot to a dash.

The machine has been "on" about 2,900 hours and during this time about 190 tube failures have occurred. However, it should be remembered that the machine has "grown" during this time and only about 1,000 of 2,700 tubes have actually been in service during the full interval.

The cathode-ray tube life is inadequately noted by our system because of the selection process which has been in progress.

Conclusion

The work on the ORDVAC started in the spring of 1949 and has been supported by a contract from the Ordnance Department for $250,000. The University of Illinois has provided a comparable sum which is to lead to a second machine. The Ordnance contract was concluded on October 31, 1951 and since that time the ORDVAC has been under test. It is currently expected that it will be moved to the Ballistic Research Laboratories at Aberdeen about February 1952. Its presence at the University until then allows a further understanding of its operation and use, and aids in the work on the machine for the University of Illinois.

References

1. Preliminary Discussion of the Logical Design of an Electronic Computing Instrument, **A. W. Burks, H. H. Goldstine, John von Neumann.** Institute for Advanced Study (Princeton, N. J.) June 1946.

2. A Storage System for Use with Binary-Digital Computing Machines, **F. C. Williams, T. Kilburn.** *Proceedings*, Institution of Electrical Engineers (London, England), volume 96, part II, number 50, April 1949, pages 183–200.

Discussion

Charles Corderman (MIT): First, speaking of the tubes you have in the ORDVAC, what is the consistently obtainable read-around ratio, and of the tubes that do not show flaws, what is the average read-around ratio?

R. E. Meagher: We usually do not check the average read-around ratio because the lowest read-around ratio is the one which would limit the use of the machine. Testing any one address may give read-around ratios of several hundred, but we have to impose an operating limit of something like 16, at this time.

David Mayer (Philco Corporation): I would like to ask for a definition of "read-around ratio". My second question is, are you using crystals in the machine? Third, how do you perform your division and subtraction operations?

R. E. Meagher: If the read-around ratio is "n", it means that we can write a dash or read a dash "n" times at that particular address without causing an error at any nearby address or any other addresses. That means when I say the read-around ratio is 16, there is some address on some tube which will fail when you hit it 17 times. We have no crystal diodes at all in the machine.

Division is carried out in the machine by a

process which may be thought of as being the inverse of the multiplication process which you saw. If we confine our attention to the division of one positive number by another, then at each step of the process we form a partial remainder which is held in the accumulator. At the beginning we have the dividend in the accumulator. We subtract the divisor from the partial remainder to form a new partial remainder. If the sign of the difference is positive, the new partial remainder is the difference shifted left one place and the quotient digit is a 1. If the sign is negative, the new partial remainder is the old partial remainder shifted left one place, and the quotient digit is a 0. The quotient is shifted with the accumulator, and digits are inserted at the right.

Design Features of the ERA 1101 Computer

F. C. MULLANEY

THE ERA 1101 computer is a single-address binary-system parallel computer using magnetic drum memory. The word length is 24 binary digits, equivalent to seven decimal digits plus sign. The logic is quite conventional.

A machine instruction consists of an operation code plus one execution address. The execution address usually specifies the location of an operand or the place where a result is to be stored. There are a total of 38 different operations which may be grouped as follows:

Ten arithmetic operations, including regular and special additions and subtractions, divide, and multiply.

Thirteen "insert" or transmissive operations.

Four "jump" or transfer operations to allow interruption of the instruction sequence in progress.

Four manipulative aids such as logical multiplication.

Two shifting operations, each shifting left one of two registers.

Two output operations; print and print punch.

Three stops; optional, intermediate, and final.

The memory element is a magnetic drum with a capacity of 16,384 words, each 24 binary digits long. The drum, which is $8^1/_2$ inches in diameter, rotates at 3,500 rpm. The resulting surface speed of 1,600 inches per second, together with a peripheral spot density of 80 per inch, produces a basic pulse rate of 125 kc for the memory section of the machine. Although the random average access time is 8 milliseconds, an average access time of less than 1 millisecond can be obtained by placing the orders and operands in locations on the drum which will permit a number of references in the same drum revolution.

The arithmetic section consists of the "X" and "Q" Registers and the Accumulator. The "X" Register, 24 bits long, functions as the repository for multiplicand, divisor, augend, and subtrahend. The "Q" Register, also 24 binary digits in length, possesses shifting properties. This register contains the multiplier during multiplication and the quotient after a division. It also may be used as a rapid-access 1 word storage. The principal arithmetic register, and the place where the actual arithmetic is performed, is the 48-place Accumulator. It possesses subtracting and shifting properties.

The number representation is in a one's complement system in which the highest order binary digit designates the sign of the number. Negative numbers are represented as complements on $2^n - 1$, where n is 24 or 48 depending on which register contains it and on whether single or double precision operation is being used.

The basic clock rate at which the control and arithmetic systems function is 400 kc. The time necessary for addition or subtraction is 96 microseconds. This time includes procurement of both operands and the next instruction from the magnetic drum memory and assumes that the drum addresses are placed to obtain minimum access time. The corresponding time for division is 415 microseconds and for multiplication, 352 microseconds.

The computation and control sections operate asynchronously with respect to the memory. Once a storage reference has been initiated by main control, further action in this section is suspended until a "resume" is signalled by the control circuitry of the memory system.

The main sequence control receives the operation code and issues the necessary operation pulses to perform the main steps involved in the particular instruction being processed. To control the more complex arithmetic operations, such as shift, multiply, and divide, an auxiliary control system is employed. It is known as the arithmetic sequence control.

The machine may be manually controlled from two locations. The operator's control panel contains a minimum number of controls and indicators for operating the machine. The maintenance control panel contains a complete display of indicators and a sufficient number of switches for complete control of the equipment for test and trouble diagnosis.

The input medium is a photoelectric paper tape reader. Standard 7-channel perforated paper tape is used, six channels of which are used for information. Four lines, therefore, contain a 24-bit word. The seventh channel contains the coded loading instructions. This code is used to direct the operations necessary to assemble the 6-bit word pieces into the standard 24-bit size, and store them in the proper location on the magnetic drum. The loading rate is 35 words per second. At this rate, the entire drum could be loaded in less than eight minutes if desired.

The output section consists of an electric typewriter and paper tape punch. The maximum output rate is about seven characters per second.

The machine logic, while not basically novel, has certain distinctive features which are worthy of mention. Two

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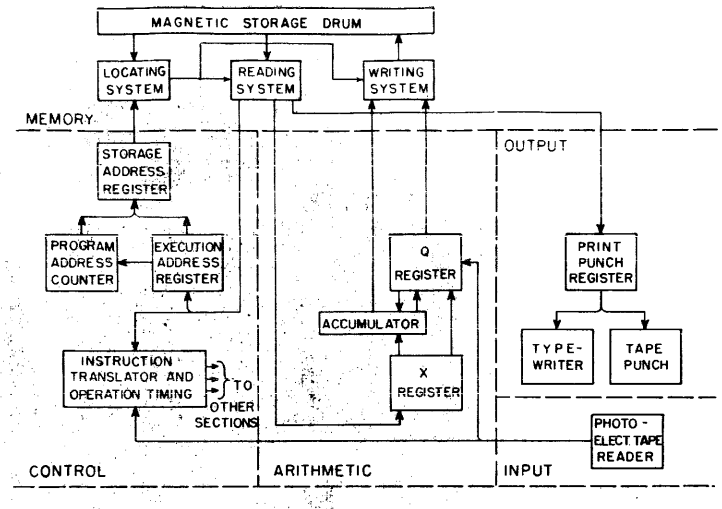


Figure 1. Principal elements ERA 1101 computer

types of multiplication are provided: clear multiply and hold multiply. In the former, the factors are held in the "X" and "Q" Registers and the product is assembled in the initially cleared Accumulator. In the hold multiply, however, the Accumulator is not precleared and the product is added to the initial Accumulator contents. This feature provides rapid performance on routines requiring the accumulation of sums of products, for example, operations on double precision numbers. Another important aspect of the machine multiplication is that the multiplier remains unchanged in the "Q" Register after the completion of the operation.

The unusually large memory capacity of 16,384 memory boxes permits long-time storage of subroutines. There is no restriction on the assignment of memory boxes to order words or operands. Either type of word is permitted in any of the locations.

Four branch operations offer unusual flexibility in programming. These operations are an unconditional jump, sign-recognition jumps, (sensing either "Q" Register or Accumulator) and a zero-sensing jump.

The output section is a potential bottleneck in most electronic computers; the ERA 1101 is no exception in this respect. However, this bottleneck can be greatly relieved if print instructions can be spaced by computational instructions. Computation proceeds immediately after the print signal is issued by the control system; the machine is not held up by output unless another print or punch is called for before the completion of a previous print operation.

The ERA 1101, with its long list of operations, provides the programmer not only with the essential tools but also many of the refinements which save programming time, reduce the lengths of programs, and result in more efficient use of machine time.

Because of the "nonvolatile" character of magnetic storage, test problems, subroutines, and function tables may be stored for as long a time as desired.

In the usual machine operation, orders are taken from consecutively numbered memory boxes as directed by a Program Address Counter. However, these consecutively numbered positions need not be physically adjacent on the drum. In fact, they may be spaced at the option of the programmer so that an operation may be completed just before the next order enters under the reading head. The operand used with an order may be so located on the drum that it is available just after the order has been read out of storage. In this way, it is possible to reduce greatly the access time which would be required on a purely random basis. Improvements in operating time of ten to one over a random arrangement are realized in practice.

Figure 1 shows the relationship among the various elements of the machine. The storage drum is shown at the top with its locating system, writing and reading circuits.

To read out an instruction, the address is transmitted from the Program Address Counter to the Storage Address Register. The locating system finds the proper address and the instruction is sent from the reading system to the control registers—the operation code to the Instruction Translator and the single address to the Execution Address Register.

To read out a number, the execution address is sent to the Storage Address Register; the number is read into the "X" Register.

For multiplication, the multiplier is placed in the "Q" register, the multiplicand in the "X" register. The product is assembled in the Accumulator. After the multiplication, the multiplier remains intact in the "Q" register. In division, the dividend is placed in the Accumulator, the divisor in the "X" register. The quotient is assembled in the "Q" register, leaving a positive remainder in the Accumulator.

Additions and subtractions are made from the "X" register into the Accumulator. Note also that 2-way communication exists between Accumulator and "Q" register so that "Q" may be used as a rapid access one word storage.

A third path from the reading system is to the Print Punch Register. The typewriter (or typewriter and punch) is energized by the output of this register.

The drum is initially loaded from the photoelectric tape reader via the "Q" Register where the word is assembled.

Constructional Features

Figure 2 is an over-all view of the computer. The cabinets to the right contain the electronic equipment associated with the magnetic drum memory. The cabinets to the left contain the arithmetic and control sections. In the center and behind the front row of cabinets is the maintenance control cabinet which con-

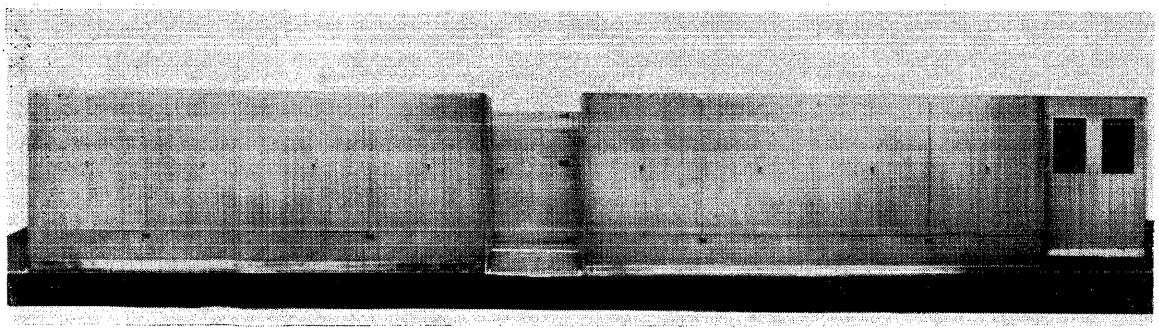


Figure 2. ERA 1101 digital computer

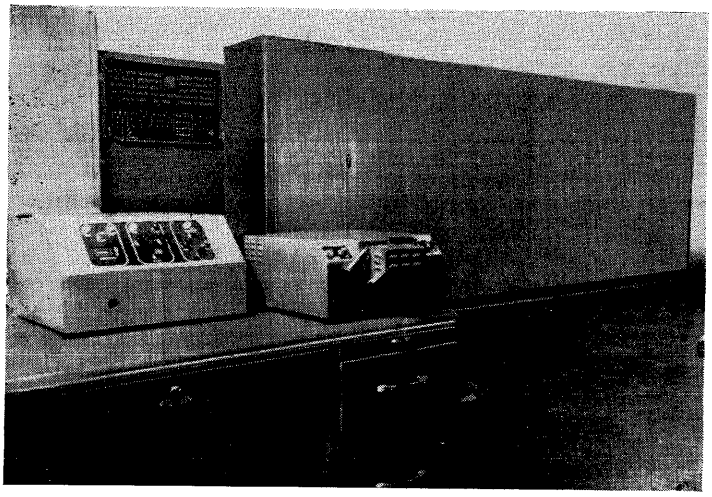


Figure 3. Portion of ERA 1101 computer

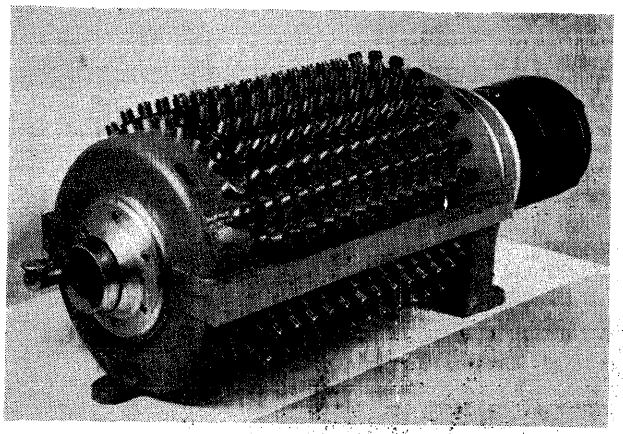


Figure 5. 400,000-bit magnetic storage drum

tains the controls and indicators used in test and maintenance of the machine. The power supply is located immediately behind the arithmetic and control cabinets. The magnetic drum is behind the cabinets to the right. At the extreme right is the fan cabinet which provides water cooled air to the other units of the equipment.

Figure 3 is a view from the operator's desk. The operator's control unit and the photoelectric tape reader may be seen in the foreground.

The magnetic drum is shown in Figure 4 with the heads in place and the cables attached. A 1/3-horsepower motor is directly coupled to the drum shaft. This drum accommodates over 200 heads and will store more than 400,000 binary digits.

Figure 5 is another view of the drum. The staggering of the heads to allow a center-to-center track spacing of 1/16 inch is shown. An integral part of the head is a 5-pin connector.

A view of one of the electronic cabinets with the door open is shown in Figure 6. The arrangement of the plug-in unit chassis may be seen. The indicators at the top are for the 100-degree Fahrenheit thermostats located in each channel. The formica spacers channel the air flow through the units and also provide protection against accidental short circuits when replacing units.

Next is the same cabinet with the chassis removed, Figure 7. The chassis engaging mechanism is shown and also the plate which contains complete identification of the unit mounted in that place.

The standard plug-in unit, Figure 8, accommodates a maximum of 16 tubes. The design allows short lead lengths from components to connector. The component boards are placed to allow effective cooling. The pan at the bottom of the unit mounts up to five dual section capacitors which are used for power supply decoupling. On this same bracket are mounted up to eight ERA molded pulse transformers. This unit size has proved to be convenient for quick isolation of a defective unit. The connectors are easily disengaged and the unit removed by means of a lever operated mechanism.

Figure 9 is a view of the rear of the Arithmetic Cabinet with doors opened. It shows the back of the channels which mount the unit chassis. The filament transformers are at the top. The heater busses and the d-c service lines run vertically. The flip-flop indicator lines and the manual control lines are laced in cables. The signal wiring within the cabinet is carried on the spaced transmission lines. Pulses leaving a cabinet are sent into coaxial cables.

The view of the front of the control cabinet, Figure 10, is of interest because its arrangement differs from that of the other cabinets. The electronic portion of the control system is shown to the left. The relays associated with the manual controls are shown here. The remainder of the space is occupied by a relay power supply and miscellaneous terminal strips.

One of the control units which contains some of the subcommand circuits is pictured in Figure 11. Note the concentration of mixing diodes on the component board.

Figure 4. Magnetic drum memory.

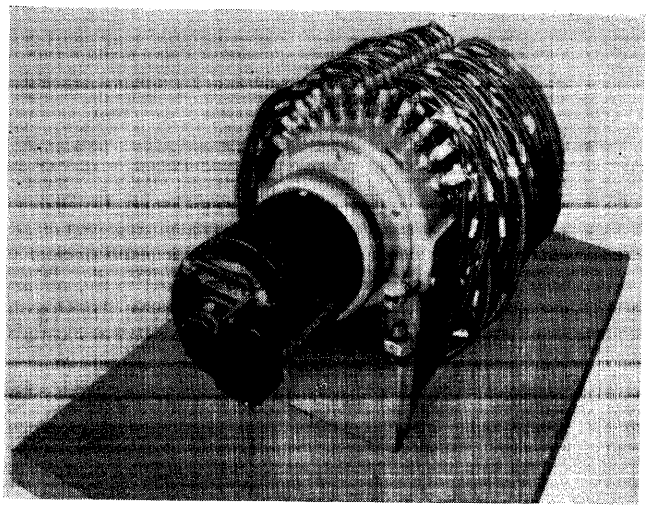
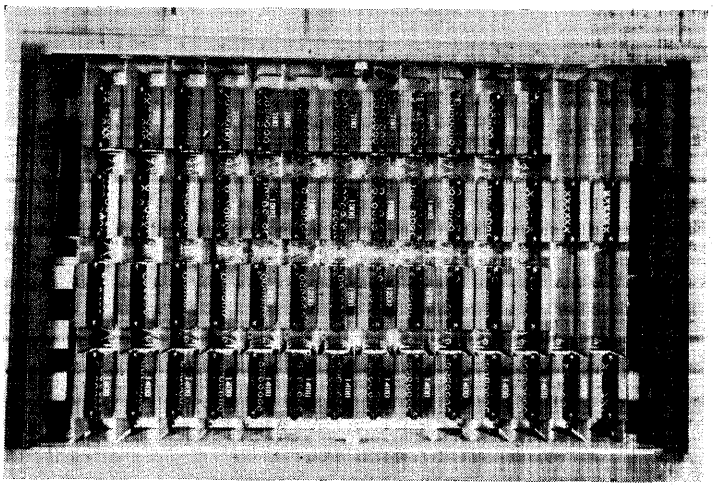
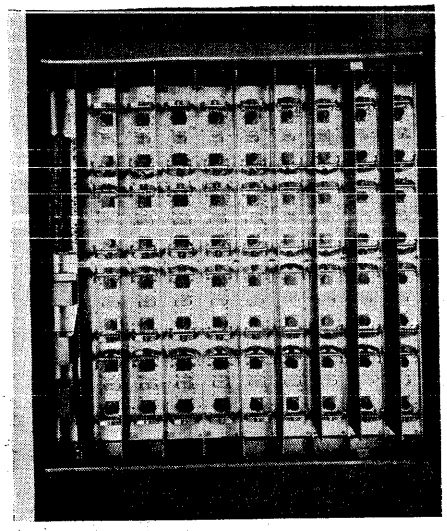


Figure 6. Electronic section of storage system





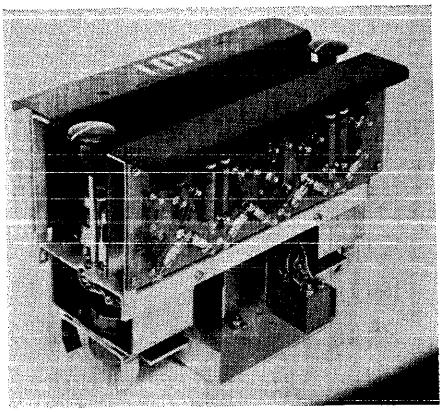


Figure 7 (left). Electronic cabinet, chassis removed

Figure 8 (above). Typical 16-tube unit chassis

In one case, for reasons of circuit design, a unit of the type shown in Figure 12 was built. It occupies on the channel the space taken by two of the smaller units. Note the pulse transformers—there are 37 in this unit.

The main control translator is shown in Figure 13. Here again, it was desirable to depart from the small size chassis. This unit receives information in the form of a 6-digit binary operation code. The information is received on flip-flops; from there on to the output, the circuits are direct coupled. There are 48 outputs built in this unit, of which 38 are used. Failure to establish an output on one of these lines at the proper time stops the machine and indicates a failure. The output, from cathode followers, is at an impedance level of about 100 ohms. The chassis contains 44 tubes and almost 200 crystal diodes.

The power control panel is shown in Figure 14, left side. It contains metering facilities, off-voltage indicators, operating and emergency controls. The section to the right contains the electronic regulators.

The cooling system consists of water-cooled air with a plenum chamber distribution system. Figure 15 shows the fan cabinet with its filters, cooling coil, and fan. The fan has a capacity of 3,500 cubic feet per minute. The water enters at 50 degrees Fahrenheit. The air is discharged into the plenum chamber at about 60 degrees Fahrenheit. The air flow in various sections of the equipment is adjusted initially by varying the size of perforations in plates depending upon the heat dissipation in a particular section. These adjustments have very little effect on the static pressure within the plenum chamber, hence any individual adjustment has a negligible effect on the rest of the system.

A closeup of a portion of the operator's desk is shown in Figure 16. On the left is the operator's control unit. It contains a minimum number of controls and indicators and allows machine operation by comparatively unskilled personnel. Having started the computation, the operator can stop the machine only at programmed stops. To the right is shown the photoelectric tape reader. The tape passes between the lamp housing and the light gate which consists of pulse shaping apertures. The light passing through those apertures which line up at any particular time with holes in the passing paper tape, impinges on the ends of lucite rods which transmit the light to miniature phototubes. A removable chassis contains amplifiers which bring the signals up to the level needed to enable the transmission gates located in one of the main cabinets.

The tape speed is 14 inches per second. The corresponding pulse rate is 140 cycles per second. If a tape snarl occurs during loading, a "tangle stop" immediately stops the drive before the tape can be snapped.

Testing and Maintenance

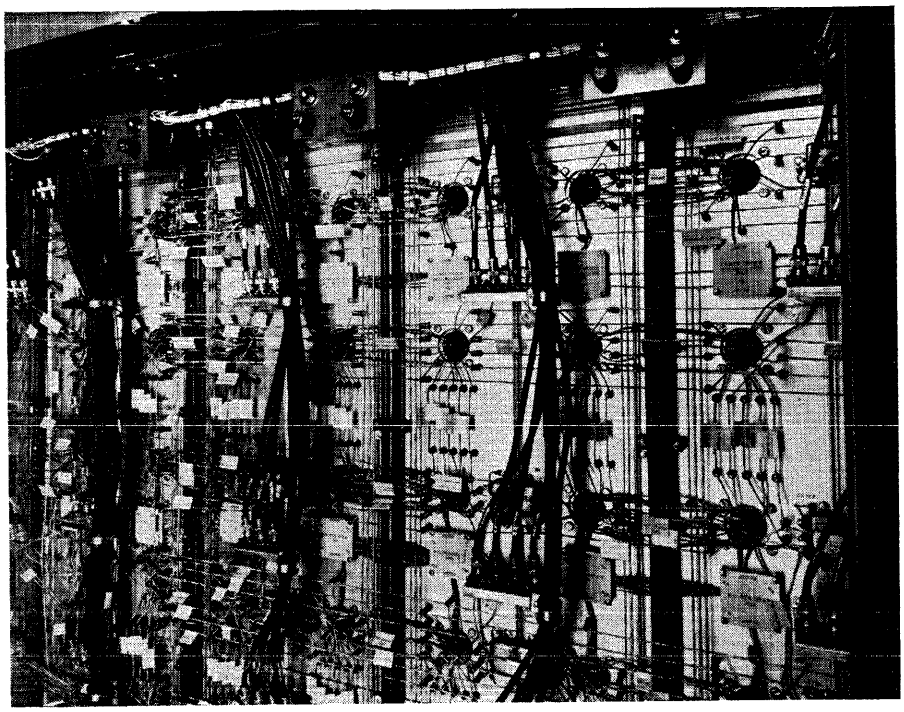
The control panel shown in Figure 17 contains the indicators and switches needed for complete control of the equipment. The machine is operated from here for program trouble shooting, testing and maintenance.

Every flip-flop has indicators on both sides. Each digit of a register has a push button for manual setting during test. One group of toggle switches allows certain control lines to be disconnected to permit cycling of normally nonrepetitive operations.

Another group of switches permits reduction of heater voltages by sections as a marginal checking aid. We do not feel that heater voltage reduction is the complete answer to marginal checking problems. It has, however, proved extremely valuable in providing a safe margin of operation. Failures rarely occur during operation.

A self-checking test problem is used in conjunction with the reduced heater voltage tests. This problem checks all of the operations used in the machine. If

Figure 9. Typical wiring in electronic sections



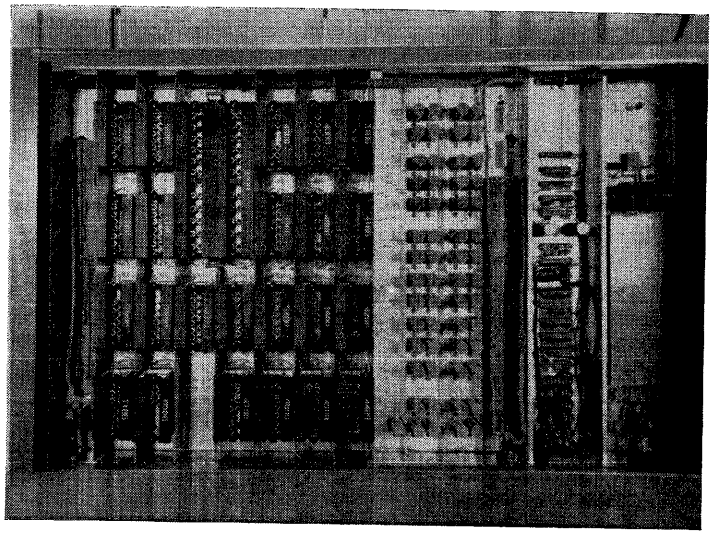


Figure 10. Control section

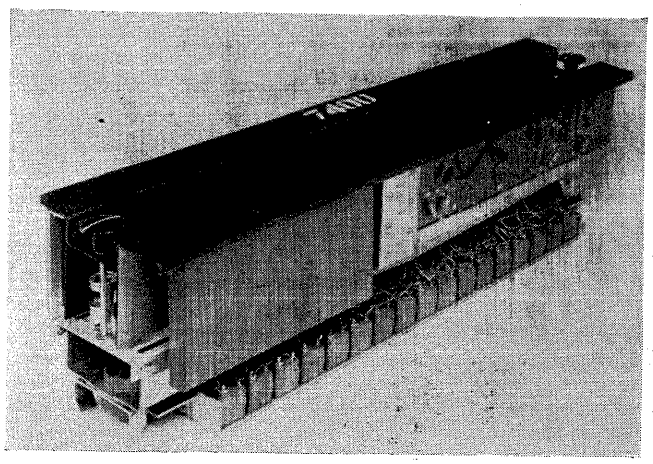


Figure 12. Unit chassis, dual size

there is a failure in any individual test, operation is halted. The address held in the execution address register at the time of the stop indicates in which test the failure occurred. Slow speed and step-by-step operation are used to pin-point the cause of the trouble.

This problem also may be used during regular operation to provide assurance that the machine is functioning properly. It is inserted automatically at intervals during the course of a computation. The time needed to execute the test problem once is about 0.1 second.

Points of circuit design which we feel contribute to reliability are: decoupling capacitors on every d-c supply line inside each chassis; cathode followers to couple flip-flops to gates; intercabinet pulses transmitted at an impedance level of about 100 ohms; pulse transformers liberally used for impedance transformation and pulse polarity inversion.

All components are operated well within manufacturers' ratings. Maximum tube dissipation is limited to 50 per cent of rating. Resistor dissipation is limited to less than 35 per cent of rating. Crystal diodes, with few exceptions, are not subjected to inverse voltages greater than half of the manufacturer's rating, nor are they required to conduct direct currents greater than 50 per cent of the ratings.

The protective features of the equipment include cabinet interlocks, air-stream monitor, and two levels of thermostatic protection in each cabinet. Each column of unit chassis contains a 100-degree Fahrenheit thermostat. If this temperature is exceeded in any of these locations, the operation is halted, but the power remains on. If the condition is corrected, the start button may be pushed and the computation will proceed. In the warmest region of each cabinet is a 120-degree Fahrenheit thermostat. If this temperature is exceeded, the machine is halted and the power is removed. Also in the category of protective features are abnormal voltage and current detectors and a drum-speed detector.

Operational Record

The computer was delivered in December 1950. It was unpacked, installed, tested, and ready for operation in only eight days. The maintenance personnel assigned to the machine are not employed by ERA nor are they under its supervision. Only two of them had seen the equipment before its delivery. The operating record being achieved is without doubt a tribute to the abilities of the maintenance group. We also believe that it speaks well for the design of the machine. For the first 4,500 hours of "heater on" time, the equipment was available operationally 86 per cent of the time. Of the remaining 14 per cent, 10 per cent was used in scheduled preventive maintenance and marginal checking. Only 4 per cent of the total time was spent in unscheduled maintenance.

A detailed tube life analysis is not available at this time. The tube replacement data which is available does not indicate outstanding life. For all of the 2,700 tubes in the machine, the survival rate at 4,500 hours is greater than 57 per

Figure 11. Unit chassis, side view

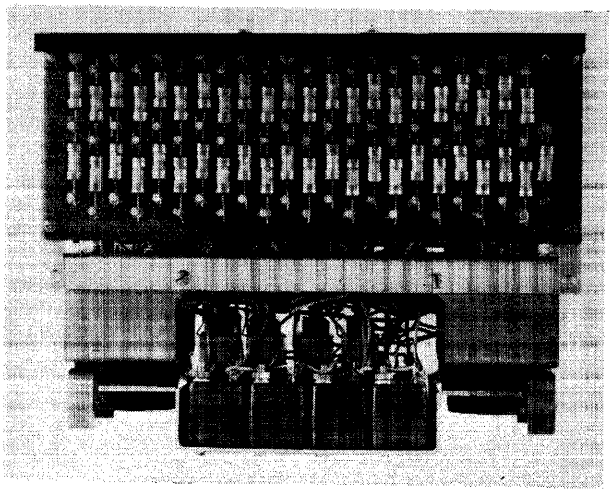
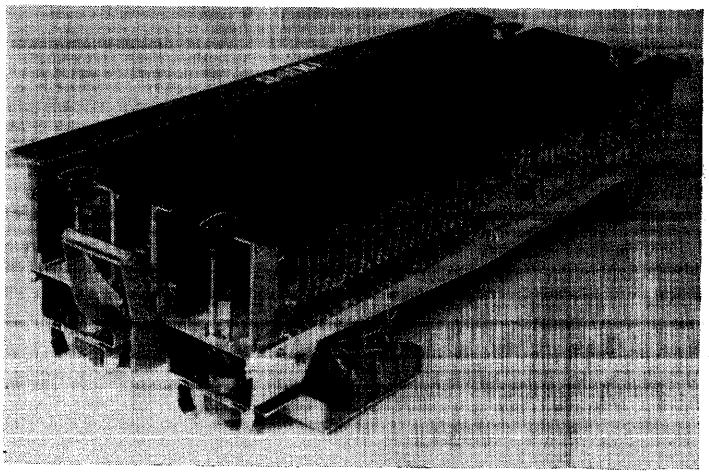


Figure 13. Unit chassis, quad size



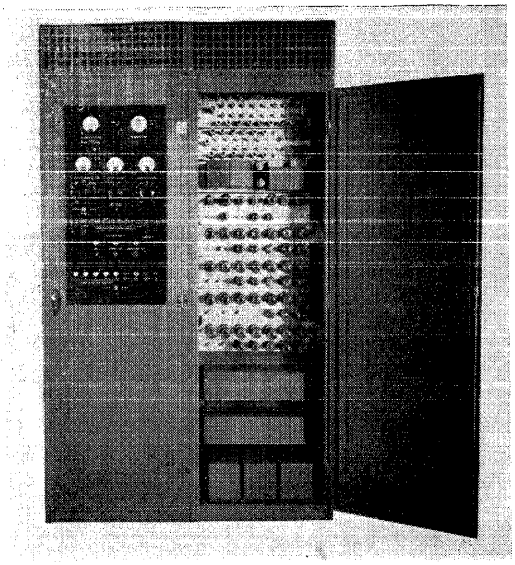


Figure 14 (left). Power supply and control

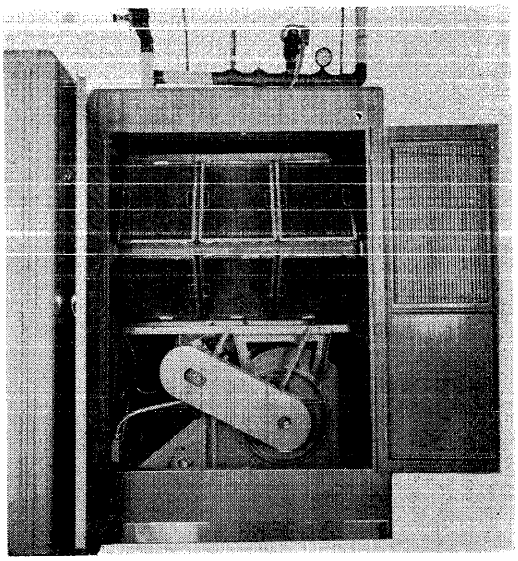


Figure 15 (right). Fan cabinet, interior view

cent. This figure does not take into account the fact that more than one tube may have been replaced in any particular socket. The actual survival figure would therefore be higher. Undoubtedly a large number of usable tubes have been replaced. The users of the machine place much more importance on the time the machine is available for use rather than on how long a tube stays in a socket. In attempting to locate some obscure fault in a chassis, all tubes may be tested. Those that look at all doubtful are replaced. It is likely that many of those replaced would have operated satisfactorily for a long time. Also, it is known that some tubes have been tested to rather exacting standards while the circuits in which they are used may be extremely tolerant as to tube characteristics. Although this type of tube replacement does not happen to agree with the procedures which we would recommend if tube life were the most important factor, the users apparently find that it produces for them the maximum amount of operating time.

Out of 2,385 crystal diodes used, 185 (or 7.7 per cent) have been replaced during the first ten months of operation. The diodes being used for replacement are of later design and manufacture than those installed originally. Their characteristics seem to be more stable than the earlier production. Therefore it is expected that the replacement rate should decrease as time goes on.

Up to this point, little has been said to indicate that there is anything undesirable in this machine. The characteristics and operational record of the 1101 make it equipment worthy of duplication. There are, of course, certain things which we would do differently in a new design.

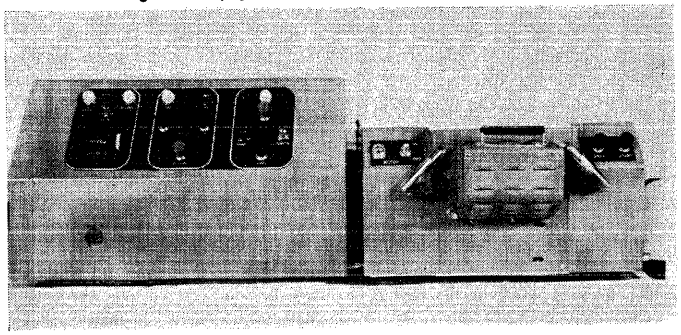
1. A new machine would have a rapid access memory, retaining the drum for a large capacity storage.
2. More extensive use would be made of germanium diodes in order to reduce the tube count.
3. Tube count could also be reduced by making greater use of a central exchange register, thereby requiring fewer transmission gates.
4. A few circuits which have proved to be somewhat critical with regard to tube characteristics would be replaced. (For example, the ERA 1101 standard pulse is 0.1 microsecond wide. A wider pulse could have been used to advantage. The greater energy content obtained would allow circuit operation with smaller amplitude pulses. Thus, the tubes can deteriorate to a greater degree before affecting operation adversely.)

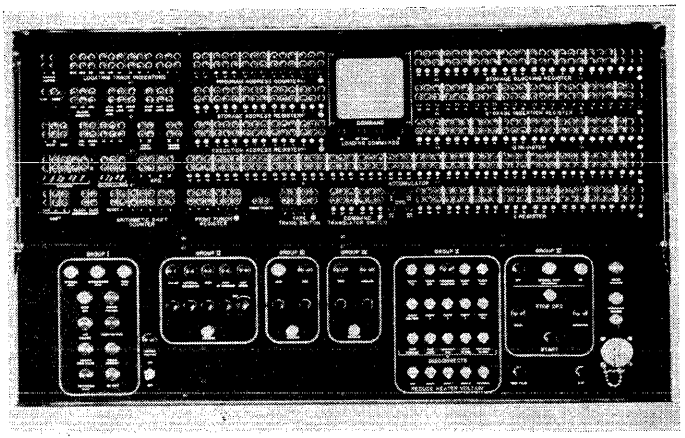
Some of the constructional features of the ERA 1101 which appear to deserve inclusion in new equipment are:

1. A plug-in chassis of about the same size.
2. A maintenance control panel. This panel could be a section of the operating console, but should be definitely separated from the strictly operational controls.
3. A magnetic drum for a large-capacity nonvolatile memory.
4. For cooling, an air-to-water heat exchanger with plenum chamber air distribution.
5. The same general scheme of protective devices as that used in the 1101: thermostats, air-flow detector, off-voltage, overcurrent protection, to name a few.
6. Conservative component deratings.
7. The general layout of the interchassis wiring.
8. Self-checking test problems plus adequate marginal checking provisions.

Figure 16 (below). Operator's control station and photoelectric tape reader

Figure 17 (right). Maintenance control panel





Discussion

G. Backus (University of Chicago): Would you be willing to estimate how soon you could deliver a similar machine?

F. C. Mullaney: That depends on a lot of things which I do not think I am prepared to state now. We are interested in duplicating the machine. We think we could do it in a reasonable length of time.

M. Rees (Office of Naval Research): "Reasonable length of time" meaning what —nine months, or four years?

F. C. Mullaney: It would be a year or so, I believe, although I certainly would not want to be held to a figure like that.

G. Backus: Will you please indicate the cost of machines of this type?

F. C. Mullaney: The figure that we have quoted in the past, and I am not sure it still holds, is about $250,000 for duplicating the machine. This does not include the accessories which comprise the output equipment and the input equipment. That is not quite as funny as it sounds, because the output equipment is standard commercial equipment; the input equipment is the photoelectric tape reader, which would add about $5,000 to the figure. That gives you a rough idea, I believe.

C. D. Cockburn (General Electric Company): You mention a 1-millisecond access time. I wonder how you spaced your orders on the drum to get this.

F. C. Mullaney: This does put a burden on the programmer. It is more difficult to program it, keeping those things in mind. We have made up a table showing the operation time for each of the 38 instructions. Knowing the time each operation takes, you will know where the drum is when the operation finishes; therefore you know the spacing of operands on the drum. The program address counter goes consecutively, but the consecutively numbered positions are not necessarily adjacent on the drum. You can change the interlace to suit the particular program on the drum.

W. J. Wachter (Moore School of Electrical Engineering): With regard to your diode life, do you make any provision for keeping the diodes separate?

F. C. Mullaney: We always mount the diodes on the outside so that they are not near the tubes. However, we do not take any particular precaution to keep them away from the resistors. Those resistors do not run very warm. We have not found that to be a problem.

H. W. Berry (Minneapolis-Honeywell Regulator Company): Does it ever happen the check problem goes through correctly but the main problem is incorrect, and, if so, can you cite some of the things that can go wrong to cause that?

F. C. Mullaney: Yes, I think so. I can speak only for the test problems we used before we delivered the machine. I do not know what the user has been doing along this line. We had a number of test problems. The one that exercised all the operations was mainly a control system check. It did not use all the memory positions nor all the possible combinations of register positions that might cause trouble, so there was a lot that did not get checked with that test problem. Additional tests were run to check each memory position and every register stage. These tests were run less frequently than the comprehensive command test.

Robert Kopp (United States Air Force): In the early part of your talk you used "precision" and "double precision." Will you elaborate on those expressions?

F. C. Mullaney: The word length is only 24 binary digits. That is a restriction in many problems. However, the instruction structure is such that it can consider the 24-bit words as pieces of larger words, and using them in this way is what I referred to as double precision operation. There are special instructions to handle these.

C. W. Adams (MIT): You mentioned that tape that goes into this machine is made up of four 6-digit characters. How do you make the tape originally?

F. C. Mullaney: It is punched three tape levels at a time. It is not a fast means of tape preparation. It was equipment that was not developed by us, which is why I am not giving more information on it.

C. W. Adams: In connection with that, does the tape stand still while you hit two different keys, or what kind of equipment is it?

F. C. Mullaney: It stands still. You hit two keys, and it fills out to six binary digits.

C. W. Adams: It is automatically switched from one to the other, then, back and forth?

F. C. Mullaney: Yes.

L. Fein (Raytheon Manufacturing Company): How long does it take you to run through each of your marginal checks by varying filament voltage, and what are the margins?

F. C. Mullaney: We allow about five minutes for the tube heaters to reach a stable condition after reducing the voltage. As we use the heater reduction, we do not differentiate between the types of tubes. We are bringing them all down about 15 per cent. Obviously, this is a compromise. We have split it up by functions of the machine, but not by tube type or function. Bringing it all down to the same value you take out a lot of tubes that might operate for a long time under normal conditions. That is one of the principal objections to the operation. It is valuable, but it is not a cure-all.

W. A. Farrand (North American Aviation, Inc.): Have you considered any other method of marginal checking?

F. C. Mullaney: Extreme filament voltage and plate voltage are the main ones we have tried.

W. A. Farrand: Are any of these worthwhile for another machine?

F. C. Mullaney: Yes, I think a combination of these things to fit a particular operation might be good.

W. A. Farrand: Concerning the photoelectric tape reader, at what rate does it operate and how much is it giving in the way of down time?

F. C. Mullaney: I do not know how much down time can be attributed to the readers. We furnish two readers so I do not think the maintenance men would let it contribute much to the down time. They would just put in the other reader. The rate is 140 characters per second.

M. H. Shuler (Consolidated Engineering Co.): I would like to know the type of diodes and flip-flop tubes.

F. C. Mullaney: We use *12AU7*'s for the flip-flops. Of the diodes, some are *1N58*, some *1N63* and some *1N34*. The *1N58*'s and *1N34*'s are being replaced with *1N34A*'s and *1N68A*'s. The "*A*'s" were furnished as spare parts with the equipment.

The Operation and Logic of the MARK III Electronic Calculator in View of Operating Experience

GLEN E. POORTE

MARK III is a large scale electronic digital computer of the serial number storage type. It contains over 5,000 vacuum tubes and over 2,000 relays. All components are of the plug-in type and are plugged into removable chassis. Each chassis is plugged into the machine by movable connectors.

MARK III is laid out in the form of a large "T". The horizontal cross bar represents the front of the machine. On this section the operator's panel, the printers, and the input-output devices are located.

In the back of the center section and extending into the vertical section of the "T" are located the sequence, storage, and arithmetic units. The storage and sequence drums are located down the center of this extension. The eight number storage drums are solid aluminum, 8 inches in diameter and 40 inches long. They are mounted in a horizontal position, and rotate at approximately 7,000 rpm. The sequence drum is a hollow aluminum casting 16 inches in diameter, 30 inches long and mounted vertically. It rotates at approximately 1,730 rpm.

The surface of each drum is coated with an iron oxide coating approximately 0.003 inch thick. Information is magnetically recorded on and read back from these drums by the use of pole pieces, the tips of which are from 0.003 to 0.005 inch away from the drum surface. The term pole piece as used in this discussion refers to magnetic reading or recording heads.

MARK III employs a coded decimal system to represent numerical data. Each number consists of 16 decimal digits plus an algebraic sign. A 4-wire bus is used to transmit decimal digits serially, with individual wires assigned weights of 2*, 4, 2, and 1 respectively. The presence or absence of a 36-microsecond pulse on these four lines determines the value of the decimal digit at any given time. The 2* and the 2 are of equal weight; however, the 2* is present only in digits of 5 or greater.

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In MARK III each line of instruction, referred to as a line of coding, is essentially a 3-address code specifying instructions for securing two operands, the algebraic sign to be applied to each, the operation to be performed and the storage location in which the results are to be recorded.

The machine has one arithmetic unit to perform additions, multiplication and transfers. It consists of an adder and multiplier. Subtraction and negative numbers are handled by taking the nines complement of the number. One addition can be performed every machine cycle which is one-half revolution of the main storage drums. The time of a half revolution is approximately 4.25 milliseconds.

The multiplier uses the left- and right-hand component technique. A multiplication can be performed every three machine cycles, and requires approximately 12.75 milliseconds for completion. The inclusion of a reciprocal subroutine makes a divide circuit unnecessary.

Other permanently recorded subroutines compute the reciprocal square root, cosine, logarithm to the base 10, exponential and arc tangent.

MARK III has a total internal storage capacity of 4,350 number values. This may be increased to any amount by using the tape read mechanisms for external storage. Of this total internal storage, 200 general registers and 150 constant registers make up fast storage. The access time in fast storage is one machine cycle. The remaining 4,000 registers are in slow storage. The access and egress time for slow storage is limited to relay speeds and is, therefore, several machine cycles. The slowness is compensated for, however, by transferring 20 numbers at a time from slow to fast storage. Slow storage selection depends upon a computed value, the sign of which determines whether the operation is to be a read or a record operation.

The function of slow storage is to store functional tables, empirical data or intermediate results.

The sequence unit is the program director. Four thousand lines of coding are available on the sequence drum.

Each line of coding has an identifying number which ranges from 0000 to 3999. Each line of coding also has 38 binary digits, the combination of which determines the intelligence of the instructions. These binary digits are known as sequence code digits and shall be referred to as such throughout the remainder of this discussion.

In normal operation, each line of coding is operated in sequence. With the aid of a line number register and a match circuit, however, any line of coding may be selected and operations resumed from that point. The transfer of control to a line other than that which would be operated in normal sequence of events is referred to as a call. This call may be made conditionally or unconditionally depending upon the flow of the problem. A conditional call depends upon the sign of a computed value.

There are eight tape-read tape-record mechanisms which constitute the input-output devices. Any one of these can be used to read information into the machine or record output on magnetic tape. Each mechanism is set by a switch to either read or record at the outset of a problem. These mechanisms record or read eight numbers per second. Only one mechanism can operate at a time, but computation can proceed while the mechanical parts are in motion. Each number is recorded in duplicate channels on the tape for checking purposes.

There are five separate printer units used for reading the recorded output and controlling the associated printers. These printers are standard Underwood electric typewriters with special solenoids for operating the keys. A plugboard and switches are used to control the typography. A printer unit prints at a rate of 15 numbers per minute, regardless of the number of digits printed from the number. There is a check circuit which compares the number printed with the number in the duplicate tape channel.

Figure 1 is a block diagram of MARK III and shows the relationship of the units, one to the other.

Although this completes the makeup of the calculator, there are two auxiliary keyboard units used with the machine. They are the coding box unit and the number tape preparation unit.

The coding unit is designed to facilitate coding operations. It is used to record the program on magnetic tape. The correctness of the program is insured by suitable checking features in the coding

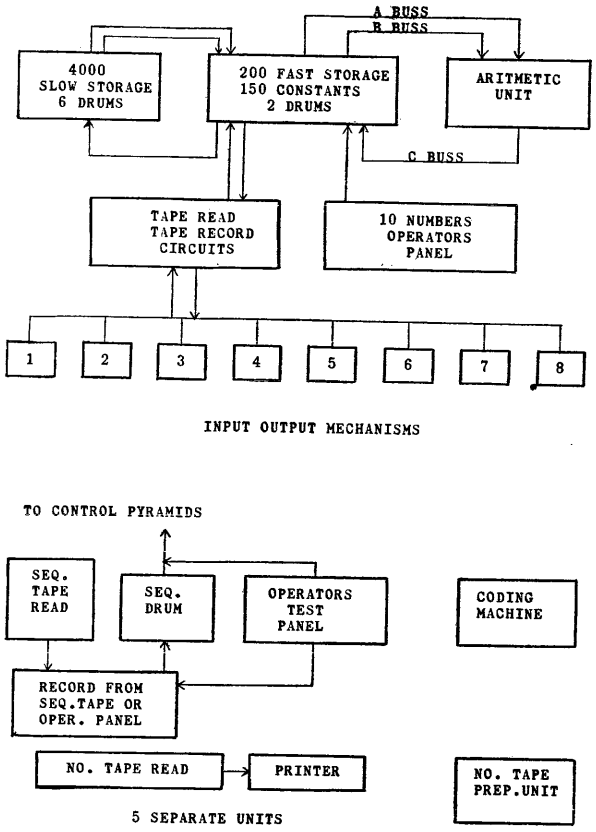

Figure 1 (left). Block diagram of MARK III

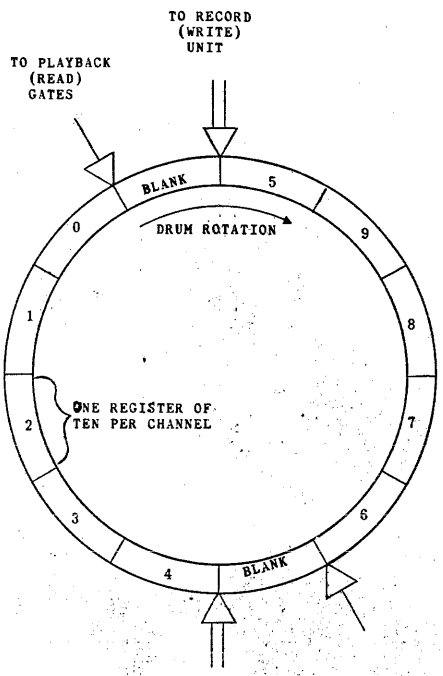

Figure 2 (right). Typical fast storage binary channel

unit. The program is then transferred from tape to the sequence drum before starting a problem.

The number tape preparation unit is used to record numerical data on magnetic tape. It also has a checking feature to insure the correctness of the numerical data. These data are then read into the calculator on one of the eight tape mechanisms.

History of Mark III

To present the background of MARK III, the troubles encountered and the problems computed, a brief history since its delivery to the Naval Proving Ground now is in order.

MARK III was shipped to Dahlgren, Virginia, in early March 1950, Reassembling and wiring checks were completed by the middle of July 1950. From last minute tests at Harvard, it had been decided that readjustments on fast and slow storage pole pieces should be undertaken. It was further decided that these adjustments should be made after shipment since damage to the drum units during shipment could vitiate the efforts if conducted prior to delivery. The purpose of this undertaking was to improve the timing of the signals and to adjust the signals to approximately the same relative amplitude for all played-back channels.

In slow storage, only the amplitudes of signals need be considered. Hence, the pole pieces were set for improved reliable read back. The improvement anticipated in fast storage, however, was not fully realized.

Concurrently, a bench experiment was inaugurated on the fast storage germanium crystal playback gating system. Considerable trouble had been encountered in this gating system because of interaction between the gating voltages. This system is a large resistor and crystal network. Hence, a change of voltage on any gating line or a change in any crystal characteristics had an effect on all other gating lines. The resulting gated signal was distorted and unreliable.

The purpose of this experiment was to determine how this could be prevented and the proper gating voltages required for error free operation.

It was found that the back resistance of many of the crystals in use was too low. Of the total number of crystals previously used in the machine, 30 per cent were found to be outside the new tolerance set for reliable operation. A new crystal with a very high back resistance was selected to replace the old one.

New gating voltage limits were determined and the circuits modified to meet these requirements. Although these gating voltages must be held to a close tolerance, the results of the gating system were much better than anticipated. Very little trouble has been encountered in the circuit since the completion of this investigation.

The work done on the arithmetic unit, following the gating system investigation, led to the design of a new playback unit for fast storage reading. The original playback unit could not accept the distorted or asymmetrical signals often encountered in the fast storage system. Furthermore, it could not handle the wide ranges of amplitude which the adjustment of the fast storage pole pieces failed to correct.

The new playback was designed for more gain but with an automatic threshold voltage to handle large signals. Provisions also were made for accepting asymmetrical signals. Here again the results were good but not as anticipated. Troubles were encountered when weak signals followed several strong signals. This has been temporarily corrected by loading the playback pole piece with resistors of values ranging from 400 ohms to infinity, depending upon the type of signals being played back.

This new playback unit has been used very successfully, however, in the slow storage system without any adjustment on the pole pieces to correct for signal shape.

During this testing period, checks were made on all chassis to determine the number of faulty components. Of the chassis checked, approximately 50 per cent of the precision resistors in the voltage divider network used in the trigger pairs and gate circuits were found to fall outside the

tolerance set for reliable operation. It is believed that these failures were a result of excessive heat in the machine. It was not until this time that the air conditioning unit was completed and put into operation. A resistor stability test was, therefore, started to determine the effects of heat. From six different manufacturers, a total of 250 precision resistors were obtained and placed in an incubator. The temperature was set at 158 degrees Fahrenheit and held there throughout the week. They were allowed to cool over the week end as was done in the machine. Initial cold values were compared with periodic readings. No failures or changes were noted during the test period of several months. These results paralleled those conducted at Harvard and are inconclusive. Only actual operating conditions can be used to determine the reliability of the precision resistors.

By January 1, 1951, all sections of the machine had been tested satisfactorily although it was realized much more work had to be done to improve the machine. It was felt that trouble would be uncovered faster under operating conditions. Therefore, a "Thirty-Second Trajectory" (time of flight) was placed on the machine and points were computed every 0.25 second.

This problem remained on the machine until the last of January. During this period of running many troubles were brought to light. First the tape-read tape-record unit functioned badly. Not only was it difficult to read tape into the machine, but it was difficult to print the recorded tape output. This condition was attributed to the tape-read tape-record pole piece timing, therefore, the tolerances were tightened. This helped but did not correct the troubles as was brought out by future operation. Second, many unexplained errors in the computed output made it necessary to rerun various values. Third, the fast storage playback gain had to be adjusted until a gain setting was found that functioned reliably for all channels of fast storage. Fourth, cross talk between the playback and record pole pieces in the partial product drum channel in the multiplier caused intermittent multiplier failures. This channel is similar to all regeneration channels in MARK III except that the pole pieces are placed closer together by approximately half the usual distance. This cross talk is the result of two affects; first, pick up which could be reduced by shielding; second, eddy currents set up in the aluminum drum. Only a degenerative feedback circuit from the record pole piece to the playback pole piece could be used to eliminate this source. We felt that shielding alone was effective enough to permit reliable operation, therefore, the feedback loop was not installed.

A pertinent point which all of this brings to light is that test routines have been helpful in analyzing trouble. But, only actual running conditions of long periods of time can be of value when evaluating the reliability of the computer units. All of the units had been thoroughly tested at Harvard and the Naval Proving Ground by using test routines. The results of these tests indicated that the units would function reliably. Only a large variation in numerical data and instructions to the machine have been found to be useful in detecting hitherto unsuspected failures. Not only has this been found to be true on MARK III but also on the Aiken Relay Calculator.

From February 1 to 28, 1951, the second problem was run on MARK III with much more success than the first. This was the fitting of equations to a drag function by the least squares method. For checking, approximately 35,000 points were computed. But, as in the first problem tape-read tape-record was unreliable and unexplained errors again occurred in the output. This required several reruns on many items.

With the aid of an oscillogram, observations were made of the signals recorded on the output tape. The signals of the numbers that failed to print were found to be crowded together. This led us to suspect either slippage of the magnetic clutch which drives the tape capstan or slippage of the tape over this driving capstan. Several things were tried to improve the operation but failed. Also, the unexplained errors in the computed results appeared to be the result of incorrect instructions. This was difficult to determine since the instructions were correct on the drum and the failures occurred only under dynamic conditions.

During the third problem, which was the calculation of a random number routine, the source of trouble affecting the instructions was traced to sequence code digit pole piece relays. These relays are used to divide the sequence drum into four groups of 1,000 instructions each. Each thousands group contains 38 sequence digit pole pieces. To change thousands groups the proper set of relays must be selected. Although the relays picked up, the contacts failed to make. If the relay was operated a second time the trouble cleared itself making the analysis of the trouble difficult.

These relays were replaced by a relay with a split or double contact. Since the installation of this new relay no further troubles have occurred due to relay contact failure.

In the meantime, work continued on the calculation of the random number routine. This was primarily a mathematical test but aided in improving the machine. It was the first problem to employ the high accuracy feature and troubles were observed when negative values were used. With a small modification in the circuits this was corrected. Several pages of output were obtained from this problem. The term high accuracy is synonymous to double precision as used in other machines.

On March 9, 1951, the random number routine was removed and a problem to compute the values of lead, superelevation and related quantities for calibration of a fire control system was put on the machine. The printed output amounted to approximately 5,000 pages.

During this period the tape-read tape-record trouble was definitely traced to the magnetic clutch. A variation of brush contact resistance on the magnetic clutch slip rings resulted in a reduced tape driving speed. This affected the relative timing of the pulses recorded on tape making it difficult to read into the machine or print the recorded output. Changing the slip rings from brass to bronze and installing a double set of brushes per slip ring has corrected this.

A problem to compute a very large number of bombing trajectories for a ballistic table was placed on the machine on June 23, 1951. It was found during this period of operating that occasional wrong calls were being made. This could not be tolerated if reliable results were to be expected. The source of trouble has not been found yet. A production time schedule and the infrequency of the failure have hampered the search. Since the source could not be located an alarm system was installed to stop the machine when such a call took place. This alarm circuit has proven invaluable to the final results.

Two and one half weeks in August were devoted to a problem involving the random number routine. Many choices as to the flow of the problem were made and a large amount of recorded output was obtained. Up to this time slow storage had been used only to store tables. But, in this problem numerical data was recorded in and read out of slow storage with very good results.

At the completion of this problem the ballistic table for bombing was placed back on MARK III. Most of the troubles encountered during this period have been

routine, the replacement of faulty components making up the major portion of lost time. We have had many high efficiency days. However, it has been found that the monthly average is low because of troubles occurring during the first part of each week. This seems to be the result of cooling the machine over the week end which causes tube and component failures. Also, while the generators and the calculator are warming up the voltages vary by a small amount but enough to cause intermittent trouble. This indicates the presence of marginal components in the calculator. These components are difficult to locate but are usually traceable to either vacuum tubes or the precision resistors used in the voltage divider circuit which I mentioned earlier. Steps are being taken to improve the voltage divider circuits by ventilating the component can and replacing the 1-watt deposited carbon resistors with 2-watt composition resistors selected for correct value.

This calculator is operated 24 hours a day, 6 days a week. The most ideal situation, however, would be to operate continuously 24 hours a day, 7 days a week.

Evaluation of Engineering Aspects

MARK III during its short period of operation has computed and printed considerable output. To some degree this indicates that the design and logic of MARK III is sound. However, as in all such machines, there are good points and weak points. These points and the associated units I shall now discuss.

Magnetic drum storage has proved to be a very reliable storage medium in the regeneration, precession, sequence, and slow-storage systems. Failures in these systems occur so infrequently that they are hardly worth mentioning. Weak tubes or faulty components in the system invariably are the source of trouble and are easily located.

Fast storage has not been included in this class because of a higher incidence of errors in read outs as compared to the other systems These failures result from an asymmetrical or distorted signal shape which gradually develops after long periods of operation. The fast storage system differs from the other magnetic drum storage systems in that each channel has two record and two playback pole pieces instead of one. These two sets of pole pieces are mounted 180 degrees apart around the drum. This procedure cuts in half the access time of fast storage by reducing the basic cycle of the machine from one to one-half revolution of the drum. The pole piece positioning is shown in Figure 2.

Since patterns are never erased on the MARK III drums but changed by recording over them it can be seen from Figure 2 that the record pole pieces must be 180 degrees apart within a very small tolerance. If they are not within this tolerance, the previously recorded signal is not completely erased when the new signal is recorded if the other pole piece is used. Hence, the resulting signal is distorted and cannot be read reliably. Furthermore, the driving current through the record pole pieces should be sufficient to saturate the pole piece core and the drum surface over a given area. As the record driving tubes age the current through the upper and lower pole pieces may differ enough to drive one but not the other into the saturation region. When this condition becomes serious enough, read-back failures occur due to the resulting distorted and asymmetrical signals. To correct this condition the *6L6* driving tubes must be rebalanced. The rate at which these tubes must be replaced for reliable operation is almost double that of the record driving tubes of other systems. This is not a serious condition but reliability and the life of many tubes could be improved by using only one record and one playback pole piece per fast storage channel at a sacrifice of speed.

Proceeding from fast storage to the arithmetic unit, the adder had been found to be very reliable. The multiplier, on the other hand, fails occasionally. The rate of failure is very low and is probably due to the interaction between the partial product record and playback pole pieces mentioned earlier. Repeating the multiplication any number of times seldom produces another failure. This may indicate that our first assumption, that shielding the partial product pole pieces was sufficient, is incorrect. A form of degenerative feed-back loop may be necessary after all.

MARK III operates with a fixed decimal point but with seven positions that can be selected by push buttons. The proper decimal point selection is always made preceding any problem. Besides the push button selection of the decimal point, any one of three coded decimal point positions may be selected. This system has been adequate for all problems thus far computed on MARK III. Not only does the fixed decimal point simplify the adder circuit but also makes high accuracy addition more convenient than with a floating decimal point system.

The tape-read tape-record troubles have been greatly reduced since the magnetic clutch troubles were corrected. Very few troubles have been encountered in the record-on-tape circuit. However, some troubles have appeared when reading tape into the machine.

It has been noted that tension on tapes in the printers causes failures due to the stretching of the plastic tape which changes the relative position of the information and timing pulses. This also appears to be the source of tape-read trouble in the tape-read system.

This effect is the result of staggering the four pole pieces on the read or record pole piece blocks. Since information is recorded or read by each pole piece, the relative timing of the pulses will change if the tape is stretched. Stretching of the tape will occur when the tape driving capstan is suddenly energized.

To correct this situation, a new pole piece block should be installed such that the pole pieces are side by side. Hence, stretching of the tape would have no affect on the relative timing of the four pulse tracks.

Investigations now being made should eventually lead to the installation of this type of pole piece block.

This brings me to the sequence unit which has functioned satisfactorily except for the trouble previously cited. I need not discuss further the sequence code digit relay troubles since that has been corrected, nor need I discuss further the wrong calls encountered while running. The remainder of the circuits have functioned satisfactorily.

Printers, on the other hand, have given considerable trouble. These troubles are traceable to mechanical failure of the stepping switches used in the system or to tape stretching troubles which I mentioned earlier. The stepping switch troubles have been corrected to some extent by purchasing replacement parts which are more rugged than the original and can stand continual operation without undue wear on the movable parts.

Another source of trouble which plagued us from the beginning was the lack of test points throughout MARK III. In the process of trouble-shooting, many connectors were unplugged and plugged as test points. Many loose connections resulted to further complicate the original trouble. During one of the early months of running, 40 loose connections were logged as the source of trouble. Since that time, every effort has been made to avoid unnecessary unplugging, and test points have been added to the machine to facilitate trouble shooting.

Evaluation of Logical Design

From the operating experience on MARK III it has been possible to obtain a good picture of the balance of the machine, evaluate the sequencing system used, and determine what circuits should be installed to increase the reliability and flexibility.

Except for a few points, MARK III is a well-balanced machine.

The rate at which tape-read tape-record operates should be increased. This could be done by reading in blocks of ten instead of one at a time. This would be time saving especially when reading in tables to slow storage. Reading both ways would facilitate the use of the tape-read unit as an external storage system on extremely large problems. It is doubtful that either of these steps will be taken in MARK III, but should be considered in future design.

This machine was originally designed with the intention of providing mathematical checks on the final results. But, it has not been possible to operate MARK III in this manner because of the frequency of errors encountered throughout the machine. Selection of the most efficient method of coding checks depends upon the frequency of errors committed by the machine. If only final results are checked, the time required for step by step checks is saved. But when an error occurs, the repeat operation is long and the exact location of the error is difficult to determine. Checking in MARK III is, therefore, accomplished by performing the operations two different ways and comparing the two results. The errors, if they occur, are then confined to just a few operations and the source of trouble quickly located.

This somewhat reduces the capacity of the machine as compared to the original intent. More fast storage could be used to facilitate trouble-shooting by retaining more pertinent information. Also, the method of coding presently used requires shrewd programming for large problems to make the best use of fast storage. Increasing fast storage would alleviate this condition to some extent and also make trouble-shooting much easier.

The work done on MARK III up to the present time indicates the capacity of slow storage is adequate and should not be changed.

With regard to the sequence instruction capacity, all indications are that 4,000 lines of coding are enough. Problems which have been computed and those that are being considered can be undertaken in 4,000 lines of coding or less. It does require intelligent coding, however, to program larger problems completely without breaking them down into sections to be done a section at a time.

These 4,000 lines of coding are stored on a separate drum unit as stated previously and are separate from the number storage. This has been an advantage since the recorded coding is never changed but only supplemented under certain conditions. Failures in the machine can, therefore, be easily divided into sequence or calculator trouble. Coding for checks in an unchecked machine, furthermore, is made easier by this form of control. The 3-address system used in MARK III also has the added advantage of supplying codes to the machine in a manner which does not deviate from the normal chain of thought.

The disadvantage of this system, on the other hand, is that the numerical data storage and instruction storage are not interchangeable. There are problems where it would be an advantage to increase the number of instructions and decrease the numerical data storage or vice versa.

These program instructions are recorded on the sequence drum with the aid of a sequence tape reading mechanism. A large program can be recorded in twenty or thirty minutes. But, due to tape reading failures, it has been found necessary to examine each line of coding after the recording process. This examination and correction of instructions requires several hours.

In view of the preceding discussion, an important fact is brought to light. In review, it has been pointed out that the fast storage capacity should be increased because of the method of checking. Also, it requires an apt person to program large problems in 4,000 lines or less. Furthermore, failures in the sequence tape reading unit cause the problem change-over time to be hours instead of minutes. It would be possible to correct this situation without changing any of the present units if the errors could be detected as they occur. This simple fact is most important, since it brings out the need for an automatic or internal checking circuit, as I shall refer to it from this point on. The people at the Naval Proving Ground do not always agree on the principles of computing machinery, but one thing they all agree on is the need for internal checking circuits. No amount of test running will indicate this. Only long periods of running and a variety of problems will convince the people of this need. Until a more reliable vacuum tube or substitute unit can be devised, the need for internal checking will be ever present.

MARK III does not have internal checking circuits yet; however, plans are being made to install checks in the sequence unit. It is hoped that internal checks on the arithmetic and storage units will follow.

Another check feature that would be desirable but which should be considered when the computer is still in the drawing-board stage is marginal checking of components. Marginal components are difficult to locate and sometimes must be left in the machine until they fail frequently enough to be located without undue effort or loss of time. Mr. Norman H. Taylor discussed marginal checking to some extent in a paper published in December 1950.[1]

Besides checking circuits in the calculator, it has been found through experience that it would be desirable to include a divide circuit, product accumulator, and both a fixed and floating decimal point which could be selected by coding. These would improve the flexibility or ease of programming.

The decision to include such circuits, however, will depend upon the amount of added equipment as compared to the features gained. The latter must outweigh the first. Since the maintenance time on any machine increases more than linearly as the amount of equipment is increased, it is always desirable to keep the equipment to a minimum.

The advantages of a fast divide unit are obvious. The product accumulator, on the other hand, would save register space and lines of instructions.

With regard to the combined fixed and floating decimal point system, the advantage of this would be to reduce the drudgery of problem analysis. Most of the work would then be shifted to the machine where it should be; also, many nonproductive operations would be eliminated.

It is doubtful that these circuits will ever be included in MARK III but should be seriously considered in future machines.

Problems Best Suited for Mark III

Since MARK III is a general purpose machine, it can handle almost all problems that might be considered material for a large scale computer. It is particularly adaptable to the solution of range tables, matrix problems, differential and partial differential equations because of its large storage capacity. Matrix problems with 60 by 60 grids or less can be solved without the aid of external storage. For grids of larger value the ex-

ternal tape storage can be used thus making it possible to compute matrix problems of even greater size. A 1,000 by 1,000 matrix now is being considered. However, this is not as complex as it may sound since there are only 30,000 nonzero elements to be considered in this matrix.

As a subclass of matrix problems, a partial differential equation in more than one space variable can be handled with ease. This is true even though a large number of functions of the variables are to be carried simultaneously throughout the problem.

Features Which Should Be Perpetuated

There are several outstanding features in MARK III which should be perpetuated in future machines.

The first of these is magnetic drum storage. The question of speed always arises when the decision for a storage medium must be made. Therefore, the fast storage medium decided upon will probably take the form of an electrostatic, sonic or other high speed media. The slow storage, however, should very definitely be of magnetic drum storage type. Also, unless a very reliable fast storage medium can be selected I would highly recommend drum storage since it has been tried and can be used with a high degree of reliability.

The advantages from the standpoint of programming warrant the inclusion of the high accuracy feature. Furthermore, the adder circuit in MARK III is such that the per cent of added equipment necessary to include such a circuit is very small. Hence, it has the added advantage of being a simple circuit to trouble-shoot.

Another desirable feature is a function sensing circuit which selects the proper constants, for use with functional computation, based upon the size of the argument involved.

A normalizing and shifting circuit also is provided for. The term normalizing in MARK III refers to the number of zeros preceding the first significant digit from the left of any number. This count is remembered and provides a control to shift the number to a new position. This control makes it possible to generalize a subroutine so it is applicable to any plugged decimal point setting.

Another desirable feature of MARK III is the auxiliary piece of equipment, the coding unit. The purpose of the coding unit is to facilitate programming. It does this by supplying many codes automatically to the tape. For example, it is only necessary to code cosine X into Y_0 if the cosine of X is required in register Y_0. The coding necessary to initiate the calls into and out of the proper functional routine and record the value X, and the results, cosine X, in the desired registers is supplied automatically. This is typical of several different operations that can be selected on the coding unit which automatically supply the coding necessary to initiate and perform them. This can be done because of the permanently recorded subroutines on the sequence drum.

Furthermore, there are several modes of operating the coding unit which provide checks on the recorded information. Included in some of these checks is a print operation which provides an added visual check. Errors detected in the coding are corrected by making the corrections at the end of the tape. This is an added advantage because tape with errors in them can be used as well as error free tapes. Hence, the demands on the coding unit operator are somewhat relaxed.

The fixed decimal point with several possible selections and the ability to stop on any line of coding are features, which to my knowledge, are unique to MARK III. The advantages of several decimal point selections are self evident. Not only does this feature reduce the nonproductive time but also increases the flexibility and ease of coding for MARK III.

The ability to stop on any specified line of coding without programming for these stops also is an advantage. This feature facilitates the program check out required by the mathematician and speeds troubleshooting. To stop on any specified line of coding is made possible by the presence of the matching circuit, push buttons and a toggle switch.

Computers in General

As a final thought, a survey of most computers in operation today indicates, in view of balance of the machine, a need for more emphasis on faster, reliable input-output devices. The term output devices as used here should include the necessary equipment to obtain the results on paper in its final printed form.

The efforts exerted in designing a computer are usually concentrated on the storage and arithmetic units. This is analogous to putting the cart before the horse since most of the difficulties in computers do not lie in these units but in the input-output systems. With few exceptions, those engaged in computer work have been successful in designing and constructing usable arithmetic and storage systems. Why then is it not possible to consider the input-output devices first and construct the remaining units around them? Until new and improved systems are devised this will probably limit the computer speeds to a relatively slow speed in view of the present devices being considered in arithmetic and storage systems. Fast computing elements, however, are of little value if long waits are encountered while the input or output device cycles.

Furthermore, computing machine speeds should be considered from the standpoint of over-all output and not on the speed of computer elements such as multiplication, addition or access times of storage media. These speeds are indeed splendid selling points but input-output and nonproductive operations must also be considered. It is possible to construct a computer of fast computer elements but which would actually be comparable in speed to the so-called slow speed computer because of nonproductive and input-output cycling time.

Failures in the faster units may also contribute to such a situation since the faster units are more difficult to construct with a high degree of reliability. It is, therefore, my contention that slower more reliable computer elements which contribute to easy programming and trouble-shooting should be selected before faster less reliable units. It is, after all, our ultimate aim to eventually design and construct a computer which can be operated and maintained by personnel who have a minimum of training and experience. At this point I feel the need to again emphasize the inclusion of internal checking circuits in future electronic computers. I believe the advantages gained will outweight the disadvantages of the added equipment.

Conclusion

In conclusion it has been my desire to present MARK III from an impartial point of view. I have attempted to neither praise nor apologize for any features. In this, I hope I have succeeded. We do realize more work must be done to improve the reliability. But, we also feel that MARK III is one of the easiest computers to program for and except for the lack of test points the easiest to trouble-shoot.

Reference

1. MARGINAL CHECKING FOR COMPUTER RELIABILITY, Norman H. Taylor. *Proceedings*, Institute of Radio Engineers (New York, N. Y.), volume 38, December 1950, pages 1418–21.

Discussion

J. Belzer (Battelle Institute): First, is it possible to read from the slow magnetic storage at the same time the machine is computing? Second, is it possible to read the results from the machine onto the slow storage drums. Third, has any consideration been given to the use of the slow storage drum as the source of printing the result rather than getting this directly from the machine, and slowing up the machine for other computation?

G. E. Poorte: First, you asked if the values could be read from fast to slow or slow to fast storage during the time the machine is computing.

Yes; normally, what we do is code the transfer of a control number to a register which sets up the slow storage relay pyramid to the proper channel. The sign of this control number determines in which direction the transfer will take place. This requires one instruction line. Computing may again proceed normally, until the laps of approximately 100 milliseconds, which is from 20 to 25 instruction lines later. This allows time for the pyramid relays to set. Only one more instruction now is required and that is the command to transfer from fast to slow or slow to fast storage. This command is the same for a transfer in either direction.

J. Belzer: Can you read computational results onto the drum?

G. E. Poorte: We can read the results of computed values into the slow storage system by the procedure described in the first answer. What was the third question?

J. Belzer: The third was whether you have considered the reading of final results from the drum.

G. E. Poorte: Not seriously, no.

J. Jankowitz (National Bureau of Standards): Can the computer modify its own instructions during the computation?

G. E. Poorte: No—only "supplement." We have in this machine an *i*-register, for example, which supplements the number time. This number time voltage selects any one of ten numbers in one channel around the drum. Since the value in the *i*-register is a computed value, any one of ten number values may be selected by one code. There are other codes that can be supplemented but the point I wanted to bring out is we do not change the coding. The coding is permanently recorded on the sequence drum.

B. Moffat (Mellon Institute): How much greater reliability would you gain in your high-speed storage matrix and reading amplifiers by using separate amplifiers for each reading head—or is there a separate amplifier for each reading head?

G. E. Poorte: With regard to fast storage channels, we have two play-back units, one for each of the two operands and we use a crystal gate network for reading back from the desired locations in fast storage.

With regard to slow storage, we have one play-back unit to handle all of the 4,000 number values which are read back through a relay pyramid.

With regard to the speed gained, I do not think such a system would be considered because the amount of equipment involved—to have a read-back amplifier for each channel—would be tremendous.

B. Moffat: I meant, would it increase your reliability?

G. E. Poorte: No, I do not believe it would increase the reliability, because I think the fast storage gating system is very reliable. I do not think we could improve it any more at this time.

E. C. Berkeley (Edwin Berkeley and Associates): What are the operating experiences that you have had on MARK III. How many hours a week do you try to operate and how many hours a week are you successful in operating—or have you not yet reached that stage?

G. E. Poorte: I did not have time to bring out percentage efficiency figures on this machine. We figure them monthly; not weekly. The monthly averages are somewhat low. One of our lowest months was 20.7 per cent efficient, and our highest 62.4 per cent. The average monthly efficiency is apparently running somewhere between 50 and 60 per cent. On a daily percentage basis, based on a 24-hour period, we have had many operating days up to 95 per cent efficient, and many, many more ranging in the 80 per cents.

B. Moffat: How much a month or a week do you try to operate?

G. E. Poorte: We attempt to operate 24 hours a day, six days a week. Maintenance time is taken only when we discover that there is trouble in the machine. We did set up a periodic maintenance check allowing the first four hours of each Monday morning for checking; by rotating around the machine we were able to pull out a number of marginal components. This was discontinued in May. Since that time we have operated continuously.

W. P. Brynes (Teletype Corporation): At what speeds do you tape-read and tape-record?

G. E. Poorte: Tape-read or tape-record reads or writes eight numbers per second.

W. P. Byrnes: What type of typewriters you use?

G. E. Poorte: The printers are standard Underwood Electric Typewriters with special solenoids to energize the keys.

W. P. Byrnes: How rapid is the printing?

G. E. Poorte: Fifteen numbers per minute, regardless of the number of digits printed per number, or ten strokes per second to be more specific.

L. A. Ohlinger: (Northrup Aircraft Company): How much does MARK III cost?

G. E. Poorte: I would say it is over $500,000.

Questioner: What was the pulse rate on slow storage and what was the mode of storage. In other words, was it binary serial, or binary parallel, or some other form of storage?

G. E. Poorte: It is 4-bit coded dedimal digits stored serially. There are four parallel wires that transmit the decimal digits serially throughout the machine. To these wires we assign the weights of 2*, 4, 2, 1. It holds for the whole machine, including instructions, except in the instructions we bring into play what we call prime numbers.

2* appears only in digits of five or greater. Therefore, a five would not be represented by a 4 and a 1, but by 2*, 2 and 1; the presence of such a 4, 1, combination in the machine would be considered a prime number. Those are used in the instructions; never in the numerical data. When it occurs in the numerical data it indicates trouble.

With regard to the pulse rate, it is the same as for fast storage. The only basic difference between slow and fast storage is the gating system employed. Fast storage gating is done electronically while slow storage gating is done by relays.

The University of Manchester Computing Machine

F. C. WILLIAMS T. KILBURN

THE computing machine which now is operating at the University of Manchester, represents the culmination of a research project of several years' standing. It seems appropriate to outline the various steps in the development of this project, since these have given the final machine its major characteristics.

The project was initiated at the Telecommunications Research Establishment, Great Malvern, at the end of the war. The development of Radar had produced many new techniques, and it was natural to seek other fields for their application. The National Physical Laboratory was already interested in computing machines, and the ACE was in its early stages.

In the United States, experiments were being made in an endeavor to store radar traces on a cathode-ray tube. Another American source reported that the observed phenomena were quite unsuitable as the basis of a computing machine store. The reason given was that the memory was too transient, and thus the record could be read only a very few times before it faded away. In spite of this unfavorable report, the application of cathode ray tube storage to computing machines was considered to be so attractive, if it could be achieved, that a research project with this as its aim was started late in 1946. Looking back, it is amazing how long it took to realize the fact that if one can read a record once, then that is entirely sufficient for storage, provided that what is read can be immediately rewritten in its original position. Experiments with a few binary digits proved that this method of storage by regeneration was possible on the screen of a cathode-ray tube, and justified further research.

In January 1947, the project moved to Manchester, but continued to have, and fortunately still has, the active support of the Telecommunications Research Establishment.

The original store used the anticipation pulse system, but since then many other configurations have been tried.[1] The one in favor at the moment is the defocus-focus system. The successful operation of a single cathode-ray-tube store containing 1,024 digits for a period of hours during the autumn of 1947 finally set the main line of the design of the machine, since from then on it was clear that it would use cathode ray tube storage.

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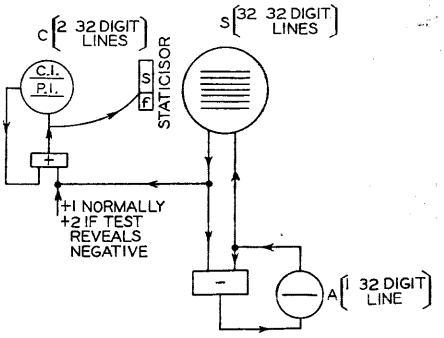
A Prototype Machine

The next development was to build a small prototype machine.[2] This machine, a schematic diagram of which is shown in Figure 1, used one cathode-ray tube as a store, S, to hold 32 words, each of 32 digits. It operated serially on the binary digits of a number, represented negative numbers by complements, and used the single address code, an instruction being of the form (s,f) where s specified a store address, and f the function to be performed. It set the tone for subsequent Manchester machines in all these respects. A second single-word cathode-ray-tube store was used as the accumulator, A, all calculations being performed by transfer of numbers between store and accumulator, while a third cathode-ray-tube store, C, held the control number recording the number of the instruction being performed. Since an instruction must be read from the store S, and must then itself control the store selection mechanism via the staticisor, each instruction must be held in temporary storage as it is read from S. A second line on the control tube, C, is a highly convenient place for this temporary storage, since the control number and the temporarily stored instruction are then both fed to the staticisor from the single source, C. The two lines of C are called the *C.I.* and *P.I.* lines, the initials referring to control instruction and present instruction respectively. Taking the duration of the sweep of one store line, that is, the number length, to be one beat, and the time taken to find, read, and obey an instruction as being one bar, this machine operated with four beats to the bar, as shown in Figure 2(A). In the first beat, S1, the control instruction was read from *C.I.*, increased by unity to cause the instructions of a program to be obeyed sequentially, rewritten in *C.I.*, and fed to the staticisor. Meanwhile the store S regenerated some line, say n. In the second beat, A 1, the staticisor selected a line of the store S and fed the appropriate present instruction to the *P.I.* line. In the third beat, S 2, the present instruction was read from *P.I.* and fed to the staticisor, while the store, S, regenerated line $n+1$. In the final beat, A 2, the staticisor controlled the store, and performed the operation specified by the present instruction. It can be seen that during beats 1 and 2 the machine was under the control of *C.I.*, while during beats 3 and 4 the machine operated in a similar manner, but was under the control of *P.I.* During the scan beats S 1 and S 2, successive lines of S, namely n and $n+1$, were regenerated, and the staticisor was set while the store was in this passive state; but during the action beats A 1 and A 2, the store was in an active state, the line scanned being determined by *CI.*. or *PI.*. via the staticisor. Basically this rhythm of four beats in a bar, which was initiated by a prepulse, has remained unchanged in later machines, though the addition of facilities of duration greater than one beat has entailed some modification after the beat A 2. This prototype machine could subtract from the accumulator, write negatively to the accumulator, write from the accumulator to the store, write to control, and add to control. It also had a test facility on the sign of the content of the accumulator, which, if the sign was negative, permitted conditional skipping of an instruction by adding 2 to *C.I.*, see Figure 1. Clearly this machine had the bare minimum of facilities, but it operated successfully on small programs in June 1948.

A Magnetic Store

Up to this point the fact that a full-scale machine with a storage capacity of about 4,000 words would call for over 100 cathode-ray-tube stores had been recog-

Figure 1. The prototype machine



nized, disliked, and forgotten. Now this problem had to be faced. Magnetic stores had, of course, been propounded for other machines in a variety of forms; wire or tape was proposed for use in conjunction with other stores and drums suggested as main stores. Wire and tape appeared to have two disadvantages. First, time would be wasted in searching for information along the medium, and secondly, some means of identifying individual digits, or blocks of digits, on the medium would be necessary. Since one objective of machine design was economy and a resulting reduction in the necessary number of cathode-ray-tube stores, it was obvious that the best solution would be one that permitted the reloading of a cathode-ray-tube store in the minimum time. The absolute minimum time is the time taken to sweep through all the digits on a cathode-ray-tube at the digit repetition rate. To achieve this it is necessary to make digits emerge from the magnetic store in exact synchronism with the sweeping of spots on the cathode-ray-tube store. This was achieved by using a magnetic drum rotated under the control of a servo system[3] that related drum position accurately to the position of a spot sweeping out the pattern on the cathode-ray-tube. This involved controlling the position of a drum rotating at about 2,300 rpm to an accuracy of about ± one hundredth of a degree, but was found to be fairly simple, granted good mechanical design of the drum. This combination of magnetic and cathode-ray-tube storage permits indefinite extension of storage capacity, by using a series of parallel tracks along the length of one drum, and by the addition of further drums. Rapid selection of any track is made possible by providing each with its own magnetic head.

With this arrangement the magnetic store becomes the major storage element, the cathode-ray-tube store being used as a sort of smoother to cut down the average rate of reference to the magnetic store to a figure appropriate to the 30 milliseconds access time of that store. One cannot be specific without considerable programming experience about the amount of smoothing that will result, but clearly with a bigger cathode-ray-tube store there need be less frequent reference to the magnetic store. Conversely more rapid reloading from the magnetics permits the use of fewer cathode-ray-tubes. There is room here for a nice economic balance, since longer access time makes possible a more economic magnetic store, but for lack of experience the optimum balance is not yet known.

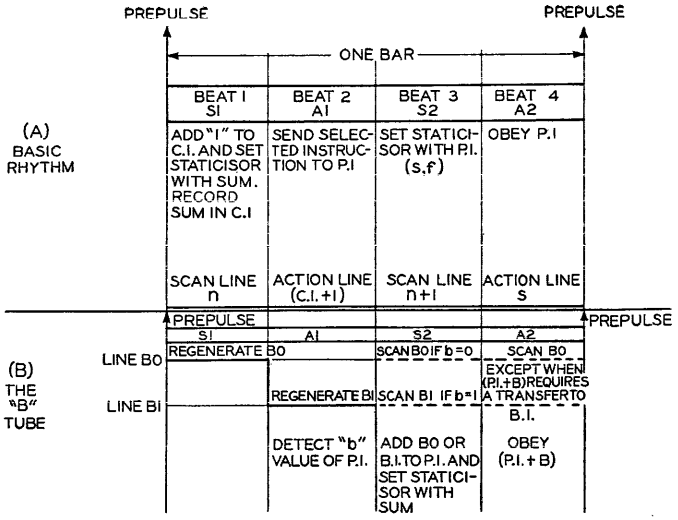


Figure 2.

(A) Basic rhythm
(B) The *B* tube

The synchronized magnetic drum was the second major controlling factor in the development of machines at Manchester and continues to provide the bulk of the storage in the present model.

An Improved Machine

Two further machines incorporating the magnetic store were built during 1949. The first,[4] shown schematically in Figure 3, was an extension of the prototype machine with more cathode-ray-tube storage, namely 128 words of 40 digits, and more facilities, including an electronic multiplier. The accumulator, *A*, had associated computing circuits for addition, subtraction and three logical operations. Multiplication involved the use of the storage tube *M*. The multiplicand was stated on the *D* line and remained there for possible further use after a product was taken; and the multiplier was stated on the *R* line. Products were added into the accumulator automatically, appropriate account being taken of the signs of *D* and *R*. Two 40-digit lines were provided for the accumulator, so that the whole of an 80-digit product of two 40-digit numbers was retained, and any rounding off required was entirely under the control of the program. Computation using the accumulator was performed modulo 2^{80}, by extending 40-digit numbers from the store, *S*, by 40 copies of their most significant digit.

The magnetic store of this machine had a capacity of 40,960 digits, but loading from the magnetic to the cathode-ray-tube store, and vice versa, could only be achieved manually. Nevertheless, during the summer of 1949, useful work was done on the machine. In particular the Mersenne numbers $2^p - 1$ were tested for primality by the Lucas test. By this means the primality of those Mersenne numbers, already known to be prime from other calculations, were checked. The values of p greater than 257 and less than 354 were also tested and the corresponding Mersenne numbers found to be composite.

A new feature, which was introduced by this machine, and which in an extended form is a part of the latest machine, was the *B* tube. This was a storage tube having two lines B 0 and B 1, either of which could be swept at will under the control of a single *b* digit in the instruction, which now took the form (*s*, *b*, *f*). The output of the *B* tube was added to *P.I.* during S 2, before *P.I.* was used to control the staticisor, see Figure 2(B). Thus instructions, and in particular their address section, could be modified in their effect without being modified in their stored form. In general, line B 0 was kept empty, so that instructions were used unmodified for $b=0$, but were modified for $b=1$. This device was primarily intended as a convenient means of drifting the effect of a whole block of instructions by a constant amount, while leaving others that were not B modified unaffected. Since then this tube has found many other similar applications. Instructions could, of course, still be modified by the more normal processes using the accumulator, but this was very often inconvenient and wasteful of time and storage space. The numbers contained on B 0 and B 1, were sent from *S* to the *B* tube by the standard transfer process, and arrived in the *B* tube during the A 2 beat.

A Large-Scale Machine

The second 1949 machine was an extension of the first, the most important development being that by which the magnetic store was brought under the control of instructions from the machine,

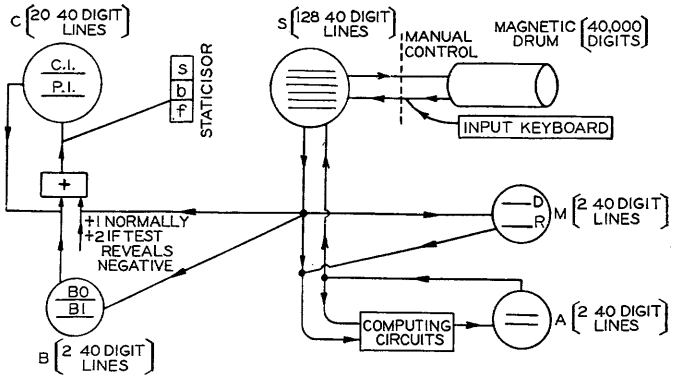


Figure 3. The first 1949 machine

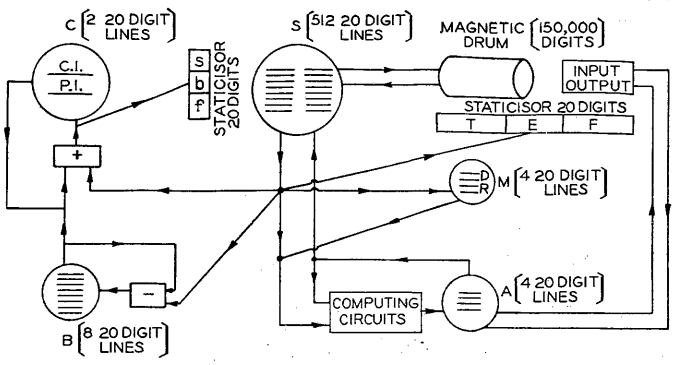


Figure 4. The present machine

reference to it being made fully automatic. The design of this facility was influenced by a desire to permit reference, not only to the magnetic store, but also to other possible stores, input and output systems, and so on, without a recoding of the machine being necessary as these further facilities were incorporated. It was also thought desirable for simplicity and economy to preserve the normal rhythm of the machine as far as possible. To achieve these results a single function, f_0, was set aside to be used as part of a standard type of instruction (s, b, f_0). In the chosen address s, as part of a program, a key word was placed, the meaning of f_0 being that the key word was to be set up on a staticisor. This staticisor was called the magnetic staticisor and it was set to the key word during the beat A 2, by the normal processes of the machine, as shown Figure 2. By suppressing the prepulse, normally given after the beat A 2, for the function f_0, the machine was then completely under the control of the key word via the magnetic staticisor. For magnetic transfers the key word took the form (T,E,F) where T stated the number of the track required on the magnetic drum, E the cathode-ray-tube store required, and F the direction of transfer; that is, whether the content of track T should be placed in the store E, or vice versa. The transfer of information took place, of course, during beats subsequent to A 2, and occupied a known time, so that a prepulse could be given after the transfer was complete, and normal operation recommenced.

In previous machines the input to the machine had been directly to the cathode-ray-tube store from a binary keyboard, and output had been by inspection of a cathode-ray-tube monitor. For this machine, input and output routines were developed which enabled teleprinter equipment to be controlled by the machine. The flow of information to and from the machine was via the last 5-digit positions in the accumulator. The routing of information between these five places, the cathode-ray-tube store, and the magnetic store was an entirely programmed procedure. This principle of using a programmed input and output, as distinct from employing special equipment, has been largely adhered to since.

A number of programs were run on this machine before it was closed down in the summer of 1950. In particular the Riemann hypothesis was investigated and verified for the range

$$63 < \left(\frac{t}{2\pi}\right)^{1/2} < 64$$

This chiefly involved calculating the Riemann function for about a thousand values of t. For this purpose the values of $\log n$, and $n^{-1/2}$ were taken from a table, $\log t/2\pi$ was calculated without reference to a table, and the cosines were obtained by linear interpolation in a table with interval $\pi/128$. The time for each term of the series was about 160 milliseconds. Further, a problem concerned with ray tracing through a lens system was investigated. The lens surfaces were spheres with collinear centers, and the rays traced were mostly skew.

The Present Machine

The machines described in previous paragraphs were entirely concerned with engineering and mathematical experiment. On the basis of experience with these machines, the design of the present machine[5] was laid down in mid 1949 and developed in detail, in close co-operation with Messrs. Ferranti Limited. A statement of the basic design principles, which also serves as a summary of features already discussed is as follows:

1. The machine, see Figure 4, contains:
   A cathode-ray-tube store using the defocus-focus system.
   A magnetic store of the synchronized drum type.
   A B tube.
2. It has a 20-digit instruction of the type (s, b, f).
3. It operates serially on the 40-binary digits of a number; the digit frequency being 100 kilocycles per second.
4. It has a rhythm based on that shown in Figure 8.
5. It has an 80-digit accumulator operating in conjunction with an electronic multiplier.
6. It uses the key word method for referring to the magnetic store and input and output.
7. It uses teleprinter equipment for programmed input and output.

These items were all, of course, included in some form in the final experimental machine, and in describing the present machine it will only be necessary to mention improvements and modifications.

Storage

Experience of the large-scale experimental machine showed that the cathode-ray-tube storage capacity of 5,120 digits was rather too small to permit flexibility of programming, and that the subsidiary storage on the magnetic drum of 40,960 digits would be quite inadequate for many problems. The cathode-ray-tube storage capacity has therefore been increased to 10,240 digits, using eight cathode-ray tubes. A typical stored pattern on a cathode-ray tube is shown in Figure 5. The magnetic storage capacity has been

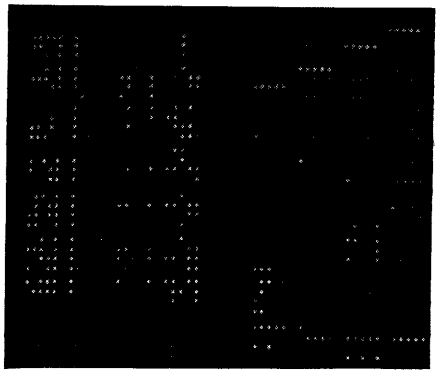


Figure 5. Typical stored pattern on a cathode-ray tube

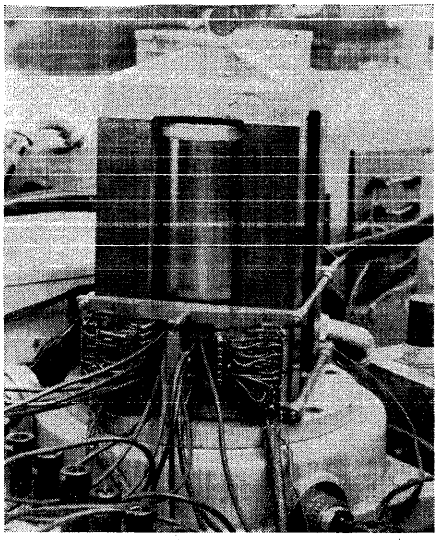


Figure 6 (left). Testing magnetic drum

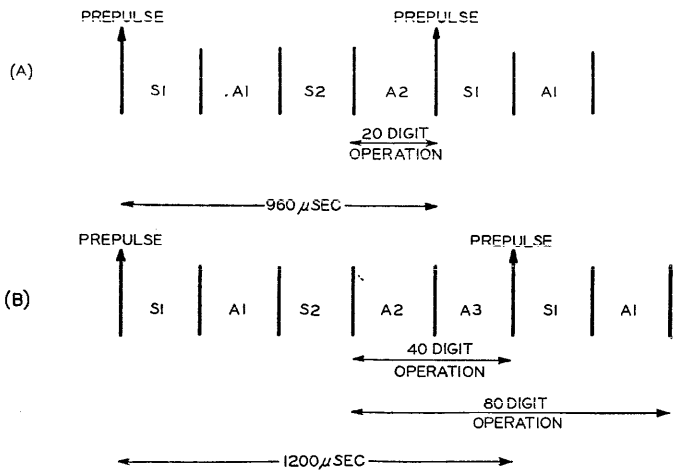


Figure 8 (right). The rhythm of the present machine

increased to 150,000 digits, provision being made for a further increase to a maximum of about 600,000 digits if this is necessary. The magnetic drum, see Figures 6 and 7, is 6 inches in diameter, and along its length of 8 inches there is sufficient space to accommodate 256 separate peripheral tracks. Each track holds 2,560 useful digits, the packing density being 165 digits per inch. Key words, 20 digits in length, cause a transfer of information between the contents of a stated track and a stated pair of cathode-ray tubes. Alternatively, if it is more convenient, the transfer of information may be between one half-track and one cathode-ray tube. In each case the correctness of transfer can be checked by a single instruction, and, in the case of an incorrect transfer, the transfer can be repeated or the machine stopped.

Selection of a particular track for reading is by electronic switching, and for writing, by relay switching.

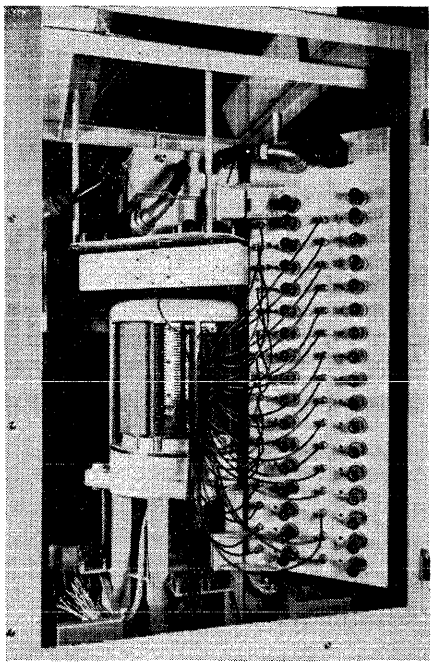
The time taken for the check, and for any transfer in which a track is read, is 36 milliseconds. For a transfer in which information is written into a track, this time is increased to 63 milliseconds to allow time for the relay switching. This discrepancy between the times for reading and writing is not important, because reading is more frequent than writing. This is so because the subprograms required during computation are all stored on the magnetic drum.

The Rhythm

To increase the speed of operation of the machine by a factor of between 1.8 and 2, the rhythm has been based on a beat whose length is determined by the 20-digit instruction, and not by the 40-digit number. This is advantageous because inspection of Figure 2 shows that, of the four beats in the bar, only A 2 is required to be of number length. Further, for operations involving the B tube and modification of the control instruction, numbers of 20-digit length only are required; so that in these cases the bar is exactly as in Figure 2, but requires only half the period of time, see Figure 8(A). For operations requiring 40-digit numbers, as for example, when the multiplicand is transferred to the multiplier tube, the bar is extended by a further action beat A 3, as shown in Figure 8(B). For those operations using the accumulator, which require an 80-digit number (a 40-digit number extended by 40 copies of the most significant digit), the prepulse is still given after A 3 to initiate the next bar.

This is permissible because only the accumulator is involved in completing the 80-digit operation, and therefore the last two beats required may be the S 1 and A 1 beats of the next bar.

Figure 7. Magnetic drum installed



The Accumulator

The facilities for performing addition, subtraction, and three logical operations have been retained, together with signed and unsigned multiplication, in which the 80-digit product of two 40-digit numbers is added to the content of the accumulator. Multiplication in which the product is subtracted from the accumulator is a new facility.

The most important engineering change of the accumulator is in the multiplying circuit. In the experimental machine the multiplication time, which depended on the number of 1's in the multiplier, averaged about ten times that for addition. A study of available programs revealed that, if this multiplying circuit were used in the new machine, about half the computing time of the machine would be spent in multiplication. Consequently, the speed of multiplication has been increased, and, in the new machine, an instruction involving multiplication is selected, interpreted, and obeyed in 2.16 milliseconds, as compared with a corresponding time of 1.2 milliseconds for addition, or any other 40-digit number operation. The increase in speed of multiplication is obtained by using a circuit consisting of a network of adders and delays, arranged in such a way that the subproducts are added together in one operation, instead of sequentially. Although some economy of equipment is achieved by carrying out the multiplication in two parts, controlled respectively by the first and second halves of the multiplier, nevertheless this type of multiplier is expensive and increases the size of the final machine by about 10 per cent. (The machine contains 1,600 pentodes and 2,000 diodes.) This, however, is judged to be worth while when balanced against the resulting over-all increase in speed of operation of the machine.

To simplify the standardization of numbers during the course of computation, an instruction has been provided

which produces in the accumulator a statement in binary form of the position of the most significant digit of any selected number in the electronic store.

An additional circuit generates, in 5.8 milliseconds, a 20-digit random number as a result of a single instruction. This instruction is used in calculations concerned with stochastic processes.

The B Tube

This facility has been improved to allow still greater flexibility and economy in programming. Eight 20-digit storage locations can now be selected by the three *b*-digits of an instruction, and thus any one of eight words may be added to an instruction before it is used.

Further, the *B* tube has been provided with a subtracting circuit, and a sign-testing circuit. Any line of the tube can therefore be used as a 20-digit accumulator for simple arithmetical processes. One important example of this is in counting the number of times that a group of instructions has been obeyed, cycling of control being conditional on the sign of a number in the *B* tube. By this means four instructions are removed from any loop in which counting is required.

The instructions provided enable a number from the cathode-ray-tube store to be written into, or subtracted from, the *B* tube; or a number in the *B* tube to be written into the cathode-ray-tube store. The line of the *B* tube involved in these instructions is stated by the three *b*-digits. To avoid the necessity for eight test circuits, one for each line, the instruction, "test the sign of *B*" reads a single circuit which is recording the sign of the content of that line of the *B* tube which was last used.

Input and Output

The input/output system is controlled by key words via the magnetic staticisor. The input uses a photoelectric tape reader capable of reading 200 5-digit characters per second. The output is by a mechanical tape punch and/or teleprinter each capable of printing ten characters per second.

The speed of input is approaching the maximum for this machine if an input program is required to organize the input information. However, the speed of output, which is 20 times as slow, can only be justified if, in general, the time of output is smaller than, or comparable with, the input and computing times together. If this proves to be untrue, an alternative scheme for input and output which has been designed around punch cards may be incorporated at a later date.

Program of Work

It is not proposed to limit the program of work on the machine to any particular type of problem, but to cover a range of problems chosen for their diversity. Thus, in the immediate future, the following items are among those which will be investigated:

1. Partial differential equations arising out of biological calculations.
2. Simultaneous linear differential equations and matrix algebra, and their application to the cotton and aircraft industries, and electricity distribution.
3. Tabulation of Laguerre functions.
4. Design of optical systems.
5. Fourier synthesis for X-ray crystallography.
6. Design of plate fractionating towers.
7. Chess problems.

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(Discussion of this paper was combined with that of the following paper)

The Design, Construction, and Performance of a Large-Scale General-Purpose Digital Computer

B. W. POLLARD

THE PRINCIPLES OF operation of the computer to be discussed in this paper have been described in the paper by Dr. T. Kilburn. The basic techniques required for the design and construction of a satisfactory computer were developed by Professor F. C. Williams and his group at the University of Manchester, and the Computer Section of Ferranti Ltd. have therefore made use of these proven techniques in their engineering approach to the problem of constructing a reliable computer. This paper describes the engineering techniques used and evaluates the performance of the computer to date, with a brief reference to the types of problems being handled on the computer. The first computer of the type described (Figure 1) now has been installed at the University of Manchester, and the construction and testing of further similar machines is proceeding.

Construction of Computer

In the development of digital computers, the point now has been reached where it is possible to produce a logical design for a computer, which will fulfill the requirements of the mathematical specification, and which can be constructed, in terms of circuits and components, with a reasonably certain expectation of success. The usefulness of a computer must therefore be entirely judged by its reliability in operation and the ease of maintenance. Consequently great importance must be attached to the mechanical design. This design must provide a very rigid base for the mounting of valve circuits with their associated components and for the interconnection of these circuits. Furthermore, the design must allow all components and valves to be readily cooled and also must allow easy access to any valve or component for testing and maintenance. It is believed that the construction of the Ferranti Computer fulfills all these requirements.

For most of the circuits a standard chassis has been used which takes a maximum of eight pentode-type valves, 27 diode valves, 66 components, a filament transformer, and 28 outlets, 14 at each end. The components are mounted on turret tags, the design of the tag strips being such that the leakage path from any tag is to earth, rather than to the adjacent tag. These chassis are mounted in doors, a typical door containing six chassis, Figure 2. The outlets on the hinge side of the door are connected via special Plessey connector strips, to flexible leads which terminate adjacent to the horizontal pulse lead ducts. The outlets on the handle side of the door are used for high-tension leads and for interconnections between chassis. The wedge shape of the chassis allows easy access to the valve bases and the inner ends of the components without increasing overmuch the size of the chassis. As the chassis are mounted in a vertical plane, there is effectively a metal sheet between the valves and the components, and hence the cooling problem is simplified. Further, the open type of chassis construction ensures that no hot spots can develop inside the chassis. When the circuit doors and the cover doors are closed the valves and the components are each enclosed in a separate chimney, so that there is a certain amount of convection cooling, which would, in fact, suffice for reliable operation. A forced ventilation system has been installed, and there is only a 10-degree centigrade rise in the temperature of the air extracted from the computer.

The swinging door type of construction gives very good accessibility to all circuits without changing their conditions of operation. This problem is simplified by the fact that all signal pulses are of at least 30 volts amplitude, whereas gate and trigger levels are of the order of 5 volts, so that small variations in capacitance or cross talk have no effect upon the operation of the circuit, Figure 3. In a serial computer of this type there is very little opportunity for the standardization of circuits and there is therefore no provision for the replacement of faulty units. It is found in practice that the majority of the time spent in trouble shooting is devoted to the location of the circuit at fault. This time is much decreased by the use of test programs, which rapidly check the operation of the computing elements, and indicate the location of any fault that is present by means of a code character, which, used in conjunction with a reference table, localizes the fault, sometimes to an individual valve, and at worst to an 8-valve chassis. Replaceable chassis would have very little effect on the maintenance time, and would certainly introduce another source of possible failures in the plug-in connectors.

For rapid checking of basic waveforms and the provision of triggering pulses for the test monitors, plug points are fitted to each door, supplying the useful waveforms.

Pulses are led around the machine in air-spaced cable ducts, there being a total of 160 such leads available. Each cable run goes from the center of a bay to the center of the adjoining bay, all junctions and interconnections being made at the center of the bays, where leads from the circuit doors are terminated. With this form of construction it is possible to standardize the construction of the bays and cable ducts and to make the interconnections specific for each bay by point-to-point wiring on numbered terminals.

The power supplies to the bays are carried on heavy copper busses along the top of the bays, and are individually fused before going to each door. The current for the valve heaters is derived from a 115-volt 1,600 cycle-per-second motor generator set, whose output is electronically stabilized. Incorporated in the electronic stabilizer is a system for slowly switching on the heaters over a period of 1½ minutes, and closing down in a similar time. With this system the heater volts are stabilized to better than 1 per cent, while the provision of multiple output transformers on each chassis ensures that there is no undue heater cathode voltage difference.

There are three main high-tension busses each of 15 amperes, at 300, 200, and 150 volts, and four low current supplies, three similar to the above, but highly sta-

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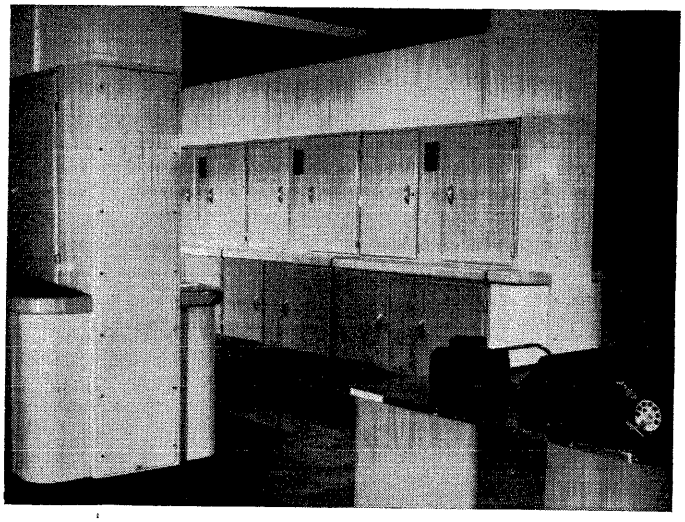


Figure 1. General view of the computer installed at the University of Manchester, with part of the control desk in the foreground

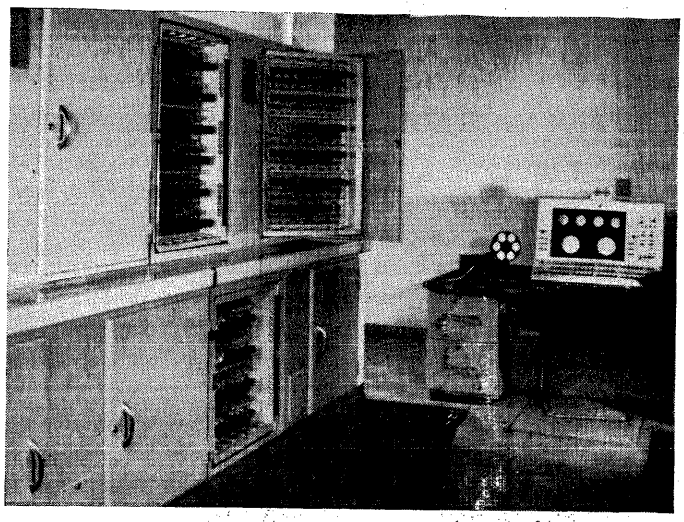


Figure 2. A view of the computer, showing circuit doors, with the control desk in the background

bilized, and a +50-volt stabilizer supply. The three main supplies are obtained from motor generator sets, with electronic voltage stabilization, and smoothed by an electronic filter network consisting of a choke with an a-c connected shunt-type stabilizer on the output. With this system the over-all stability is considerably better than 1 per cent and the peak-to-peak ripple, under machine computing conditions, is less than 0.25 volt. All power supplies, and every valve in the stabilizing system, can be metered, and the stabilizers, which are of identical construction, can be rapidly changed. The whole system is interlocked, so that the high-tension voltage cannot be switched on before the heaters, and all the high-tension voltages must be available before power can be supplied to the computer.

The Electronic Design of the Computer

The computer is fundamentally a low-speed machine, as the basic digit frequency is only 100 kc per second. High computing speeds are obtained, however, by virtue of the rapid access time of the Williams type storage system. A further advantage of this type of storage system is that the period allowed for the computing circuits to operate, sometimes known as the 'meditation' time, is accurately defined. Information is received from the store not later than 1 microsecond after the beginning of the digit period, and information must be returned to the store not later than 3 microseconds after the beginning of the digit period. Hence there is a meditation time of 2 microseconds during which the computing circuits must settle to their final configuration. As the meditation period has a mark space ratio of 1 to 4, it is possible to be quite sure of the independence of successive digits. An average 1,000 arithmetic operations per second are performed.

Because of this low basic pulse rate, it is possible to make use of the accurate bottoming characteristic of a pentode such as the *EF50*, the approximate American equivalent of which is the *6AC7*. A 'bottomed' *EF50* has an output impedance of 2,000 ohms, and it is found that all *EF50* valves bottom in the range +12 to +18 volts for an anode load of 47,000 ohms. As negative going pulses are used throughout the computer, the negative excursion is defined by the values of the level changing resistor network, whilst the positive excursion is held at ground level by a catching diode on the output of the resistor network. As a result of this simple definition of voltage levels the machine may be connected in a completely d-c manner, thereby overcoming all doubts about the dependence of machine operation upon variation of digit patterns.

When the circuit design was started it was intended to assume a 30 per cent variation in valve slope, ±20 per cent change in component value, and ±10 per cent change in high-tension voltage. It was found that although the first two requirements could be fairly easily met, it was difficult to satisfy all three requirements simultaneously. Hence, in view of the stability of the power supplies provided, designs were based on the first two requirements only. As a final safeguard 10 per cent components were used throughout the machine.

In the circuit design no attempt has been made to minimize the number of valves, or to make use of waveforms which were just good enough. In spite of this, the over-all number of valves is very small when compared with the number of facilities available in the computer. Throughout the machine all the trigger and counter circuits make use of the same basic circuit, in which the triggering and retriggering pulses are applied to the grids of the valves, and the crossover switching networks are connected to the suppressors. The suppressor waveforms are fed into cathode followers, the outputs of which are used as the output waveforms from the circuit.

Gating circuits normally use an appropriate assembly of diodes, although multi-electrode valve circuits are used in cases where fast operation is required.

In arranging the decoding of the function numbers to set up the required routes through the machine for a specific operation, there are two alternative schemes. One is to have a central decoding station, with as many outputs as there are functions, using each output to operate the required gates and circuits by means of multiple 'OR' gates. The alternative scheme is to decode at each functional gate or circuit. As many such gates or circuits have to be operated for more than one function, it is possible to save on decoders by decoding on only part of the function number, that is, the decoder may be made operative for 1, 2, 4, 8 . . . function numbers. With this system care has to be taken in the allocation of function numbers to the various functions, but that the system is economical compared with the central decoding station system will be seen from the following:

Number of functions..... 52
Number of function gates and circuits.. 53
Total number of operations for function gates and circuits, for all functions.....184
Number of decoding units in central decoding station..... 52
Number of decoders in system used.... 53

It has not been found that the latter system, which is used in the computer, has introduced any difficulty into the maintenance and testing of the machine. Although one extra decoder is required for the system adopted, the 53 decoders perform the 184 operations without any additional encoding. The more conventional decoder and encoder would have used approximately three times as much equipment.

It should be noted that no special valves or components have been used in any part of the equipment. Of the four main valve types used, the *EF50* is employed in most circuits, the *EF55*, of which the American equivalent is the *6AG7*, is a high power valve used chiefly for cathode followers, the *EA50* (*1/26AL5*) as the switching diode, and the *EF91* (*6AK5*) as the amplifier valve in the cathode-ray tube and magnetic drum storage systems. The resistors and condensers used are all standard commercially available components, the resistors being ordinary carbon 10 percent tolerance items, except in a few cases where either 2 per cent high stability cracked carbon resistors, or high wattage wire-wound resistors have been used. All components are chosen so that the mean power dissipated in them is only 50 per cent of their nominal rating. This under-rating of components, combined with the low ambient temperature, has led to very reliable operation, as will be seen from the later discussion of machine reliability. The following shows the approximate number of valves and components used in the computer:

Valves EF50..... 950
Valves EF55..... 350
Valves EA50..... 2,350
Valves EF91..... 300
Other types..... 50
Resistors.....12,000
Condensers..... 2,500

The Cathode-Ray Tube Store

The principles of operation of the Williams Storage System have been widely described, and we will only remark that the present computer uses a mixture of two types of operation—the "defocus-focus" and the "dot-dash" systems. It was found that although the defocus-focus system was to be preferred as it showed a reduction in the number of troublesome 'phonies', an increased amplitude of signal, and a reduced sensitivity to time base voltage fluctuations, it was not possible to obtain satisfactory single shot writing with the available 'digging' time of 1.8 microseconds, although the system was quite satisfactory at 5 microseconds. The addition of a very small amount of dot-dash type deflection, in which the focused dash was drawn to the edge of the area defined by the defocused dot, overcame this problem, and this method of operation has been found to be very reliable in practice.

Special cathode ray tubes are used which have several unusual features. The electron gun assembly, which is of the pentode type, is specially designed to give a finely focused beam at low accelerating voltages. At 1 kv on the final anode, the focused spot size is 0.3 millimeter. The alignment of the gun, and the assembly of the deflector plates is carefully controlled, the specification allowing 5 millimeters variation in the position of the undeflected spot from the center of the tube, with an X sensitivity of

$$\frac{660 \pm 80\text{mm/v}}{V_{a3}}$$

and Y sensitivity of

$$\frac{1{,}100 \pm 120\text{mm/v}}{V_{a3}}$$

These relatively close tolerances allow the tubes to be operated in parallel from the same time base systems, without reducing unduly the usable screen area, which measures 10 centimeters × 10 centimeters on a 6-inch cathode-ray tube. On this area are stored 1,300 digits on 65 20-digit lines, although on test 2,560 digits have been stored on the same area. The phosphor of these tubes consists of a thick layer of carefully purified Wille-

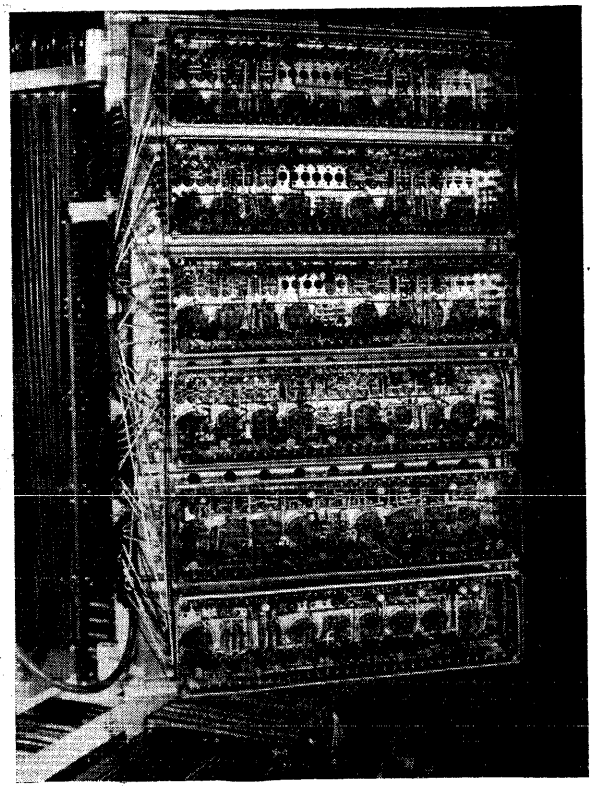


Figure 3 (left). One of the chassis doors, showing typical circuits and interconnections

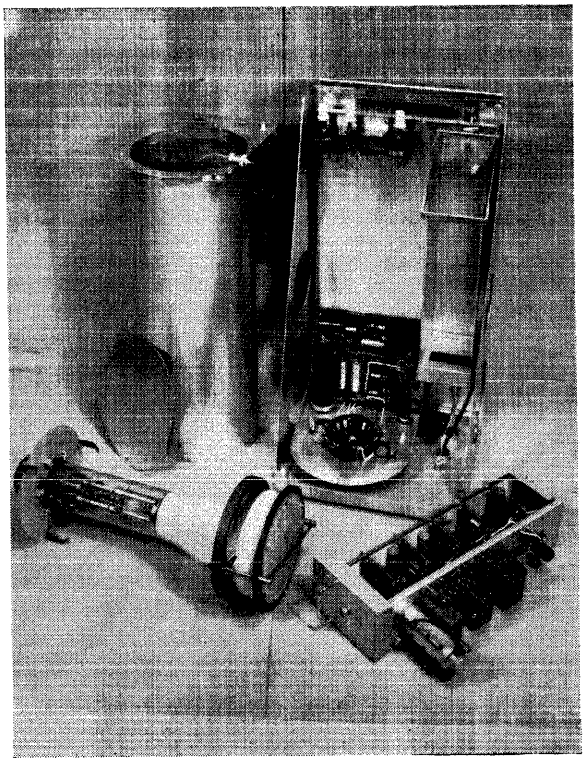


Figure 4 (right). The component parts of the cathode-ray tube storage unit

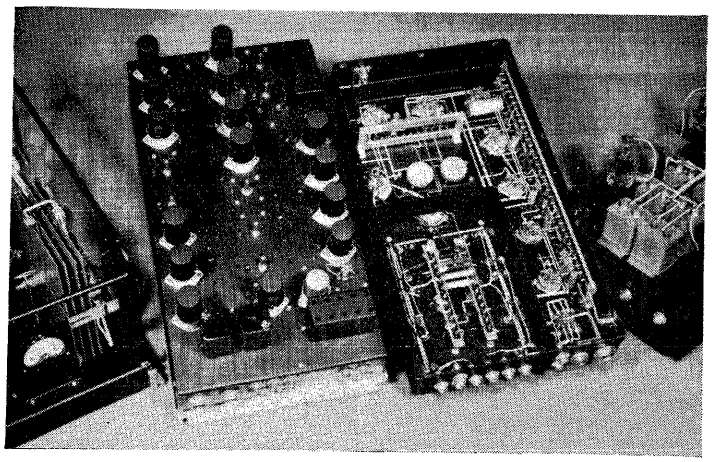


Figure 5. The timebase and stabilizer units

mite. The layer is made thick to overcome pin hole problems, and careful purification reduces the number of 'phonies', that is, points where the phosphor has an abnormally low secondary emission characteristic. The use of a silver coating as an inner conductive deposit instead of the more normal aquadag also helps to reduce the number of phonies.

The cathode-ray tube storage unit, Figure 4, comprising the cathode-ray tube assembly and amplifier, is enclosed in a shielded box. The cathode-ray tube has a shield fitted to its base, which also is an aid to the fitting of the tube into its socket. The pick-up plate is clamped against the face of the tube by means of a sponge-rubber-covered ring around the flare of the tube. This assembly fits into a double screening tube the inner cylinder of which is mumetal, and the outer mild steel. After the tube is in position a front panel is fitted to the shielding tube. The cathode-ray tube shield is grounded at one end only, to prevent circulating currents, and the amplifier is placed immediately alongside with a very short lead from the pick-up plate to the first stage grid. This amplifier, which has a pass band of 5 to 750 kc per second, is of fairly conventional design except for two features. It has been found that many so-called low-noise amplifier valves produce sporadic pulses of the order of 1-2 millivolts more frequently than would be expected from ordinary noise theory. Two valves which show an improvement in this respect are the *EF37A* and the *M.E. 1400*, the latter being used for the first stage. The other feature of this amplifier is the introduction of a delay line into the cathode of the penultimate stage. As the time constant of the first grid circuit is long compared with the digit period, asymmetric waveforms are produced in normal regenerative operation, with consequent dangers of shift of zero level, and movement of the grid base. The introduction of the open circuited delay line makes the normal regeneration signals symmetrical and reduces the asymmetry of the waveforms produced when writing is taking place.

The extra-high-tension unit, the time bases, and the time base high-tension stabilizers are special units, Figure 5. The X and Y time bases, in the center, are antivibration mounted, and are supplied with carefully smoothed high-tension derived from a stabilizer, part of which is shown on the right. The extra-high-tension unit is not regulated, but is derived from the stabilized 115-volt 1,600 cycle-per-second supply. Part of this unit is shown on the left of Figure 5. The high-tension stabilizers are of an a-c type, as variations in voltage at frequencies less than 5 cycles per second are unimportant. The amount of ripple permissible on the time bases is 20 millivolts, and the peak-to-peak ripple on the output from the stabilizers is less than 10 millivolts.

On test, storage patterns have been stored for periods of up to 40 hours without error, and the cathode-ray tube life appears to be at least 12,000 hours,

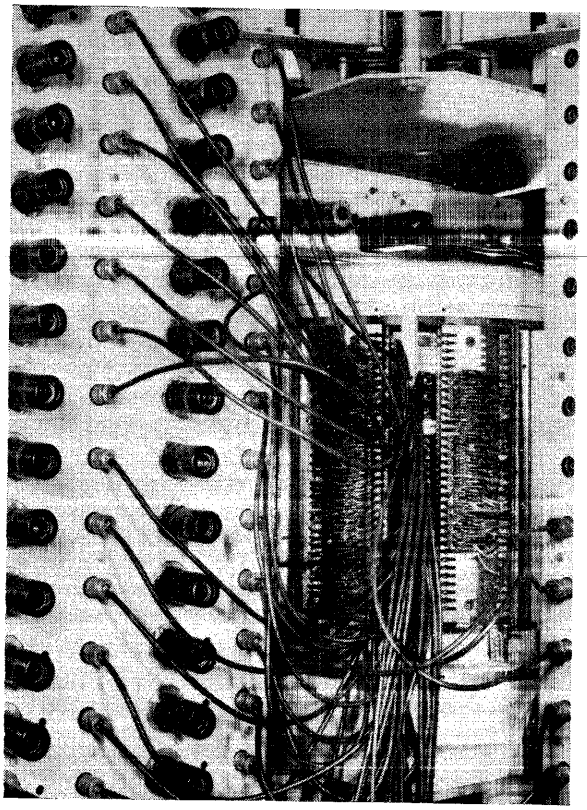
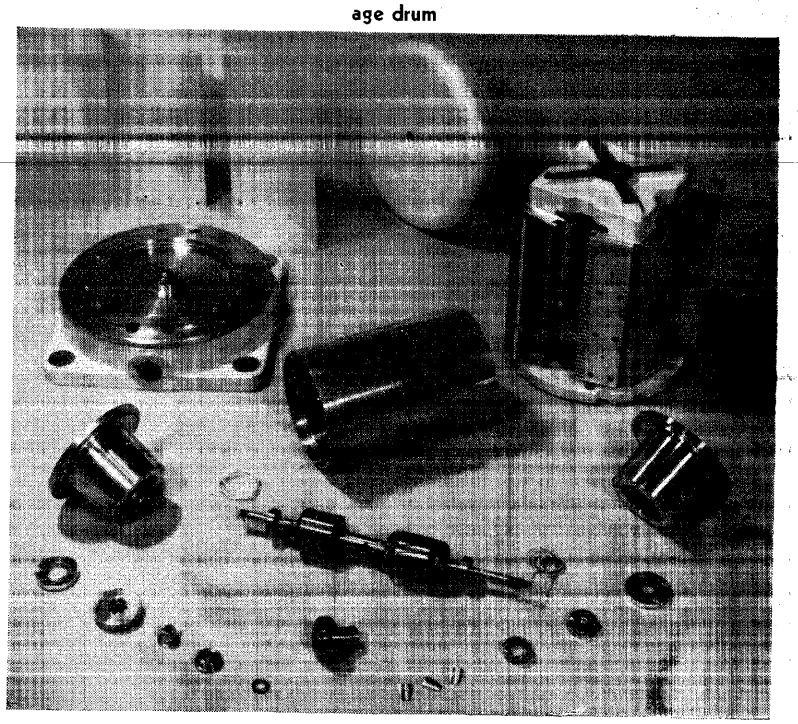


Figure 6 (left). The magnetic storage drum and associated equipment installed in the computer

Figure 7(below). A detailed view of the construction of the magnetic storage drum



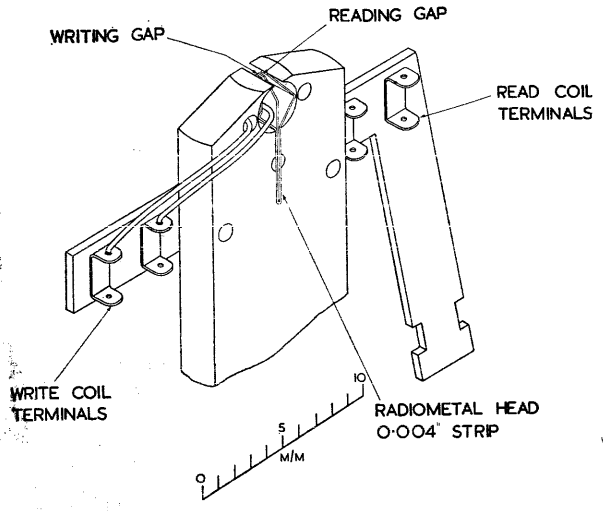


Figure 8. Schematic view of the magnetic recording head

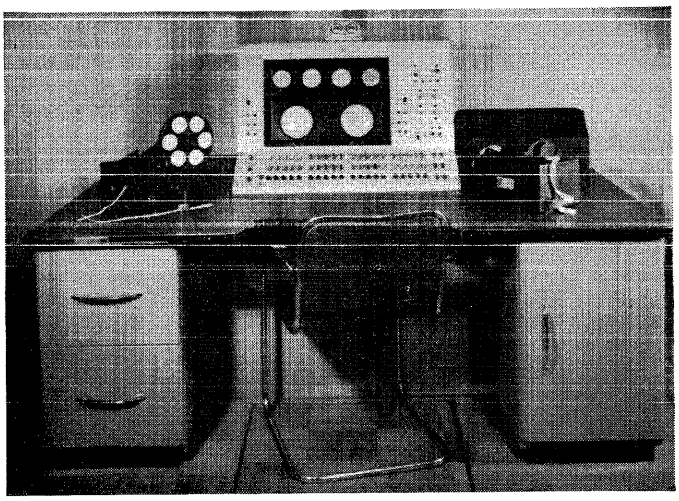


Figure 9. The control desk, with console and input-output equipment

as no tubes have failed since the computer was brought into operation. Furthermore, the stability of operation appears to be very good, as minor adjustments only have had to be made to three of the 12 stores in operation during the last three months.

The Magnetic Drum Storage System

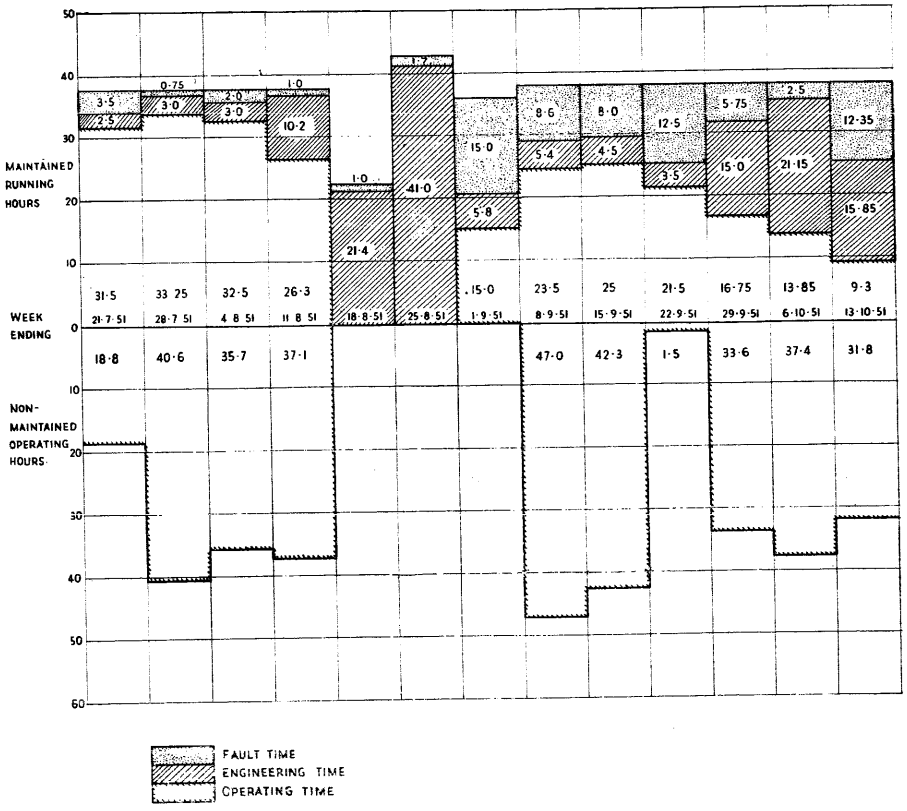
The outstanding feature of the computer is the very large backing up magnetic drum store, which may be truly considered as the main storage system. This has an ultimate capacity of 655,360 digits, or approximately 16,000 long numbers. So far a capacity of 4,000 long numbers has been installed, Figure 6.

The basic drum, Figure 7, consists of a cylinder 8½ inches long and 6 inches in diameter, driven internally by a squirrel-cage induction motor. Its normal running speed is 1,950 rpm and it has an eccentricity of less than 0.0003 inch. The drum is plated with a thin film of nickel, and precautions even more stringent than those taken in gramophone record processing have to be taken, as any impurities or pin holes in the nickel film would lead to unreliable operation. Each recording head is 0.012 inch wide, and there are approximately 170 digits recorded per peripheral inch, or 2,088 digits per track.

The drum is run in synchronism with the basic clock waveform generator of the computer, and the positional synchronising accuracy is 1/100 degree or approximately 0.0005 inch at the circumference. This accuracy of synchronization is obtained with a circuit similar to those used for "balanced strobes" in radar systems, a series of pulses recorded on the drum being balanced against a clock waveform. The total linear range of the servo is ± 1/30 degree, so that the desired accuracy is readily achieved if there is no external disturbing force. Any such force would necessarily come from the drum bearings, which are of extra precision finish, and the drum had therefore been designed with a very high inertia friction ratio to offset any irregularities in running. If a disturbing force equal to twice the normal running friction is assumed to be dangerous, then it may be shown that an inertia-friction ratio leading to a run down time to standstill of 23 minutes is necessary. The drum in use has a run down time of over 30 minutes, so that there is a considerable margin of safety. The braking force is applied to the drum by means of an eddy current brake, mounted on an assembly similar to the driving motor.

The recording system used is one of phase modulation in which a square wave recording current is used, the waveforms being positive or negative at the strobing time dependent upon whether a 1 or a 0 is to be written. The advantage of this system is that the waveform is balanced about zero, and hence no d-c component need be considered in the design of the transformers associated

Figure 10. Graph showing the operational performance of the machine to date



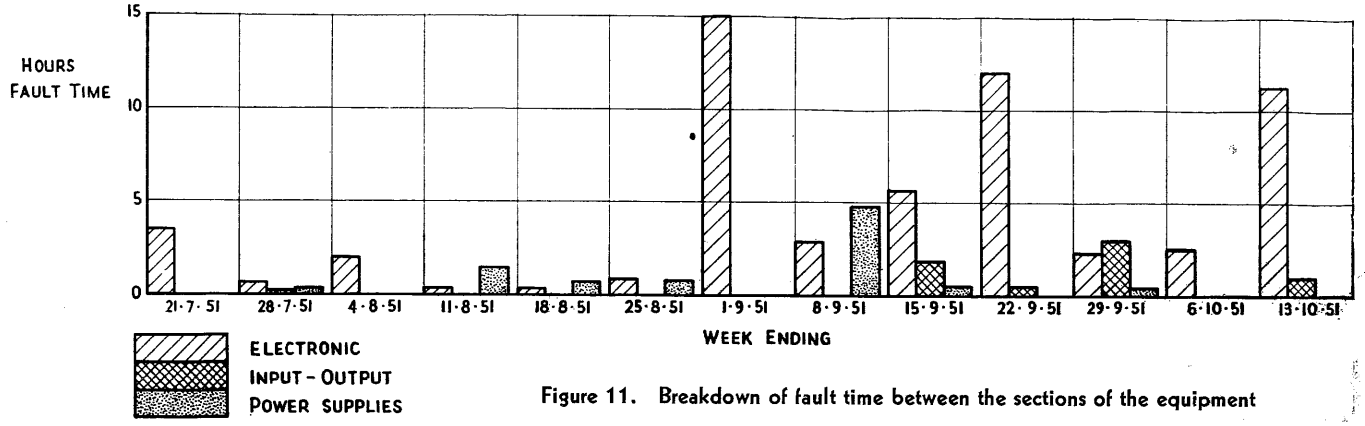


Figure 11. Breakdown of fault time between the sections of the equipment

with the reading and writing system. Since the recording is at the basic digit frequency of the machine, it is necessary to provide two heads per track, one for reading and one for writing, spaced apart by rather less than one digit length. The strobe examining the input digit waveform is placed one third of the way along the digit, so that the recording waveform is 1/3 of a digit late on the input. As the peak amplitude of the output waveform is examined there is a further 1/4 of a digit delay, giving a total of 7/12-digit delay. There also is a slight delay in the reading amplifiers, so that a total delay of approximately 5/6 of a digit is introduced. Hence to restore the correct timing the reading head must be placed in advance of the writing head by approximately 0.005 inch. The method of achieving this is shown in Figure 8 which shows the construction of an individual read-write head.

There are 256 tracks on the drum, obtained by interleaving eight blocks of heads. Each head is selected for writing by means of a relay tree, and each head has a final transformer of 20:1 step down to provide the head writing current of 4 amperes. The selection of a track for reading is by means of a switched amplifier tree.

The Input Output Equipment

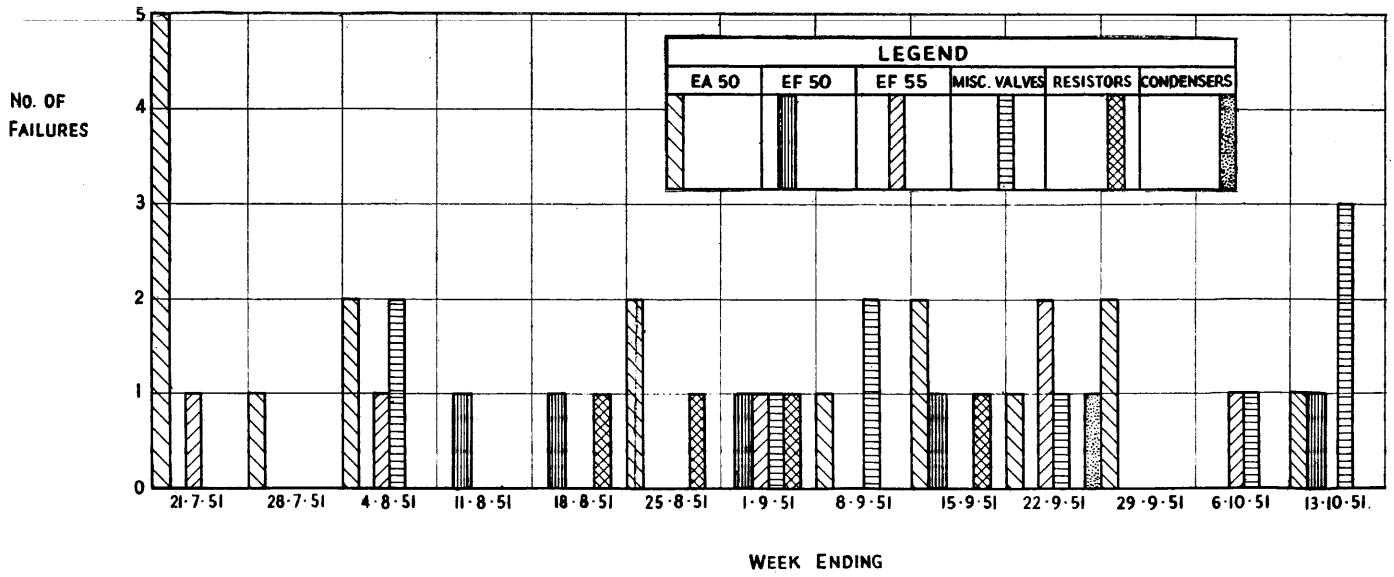
There are four units grouped on the control desk, Figure 9. In the center is the control console, with store displays, and switches for controlling the operation of the machine. On the left is the output tape perforator. In the right background is the teleprinter output, and in the right foreground the tape input unit.

The three main rows of switches along the bottom of the console are, at the top, a group whose setting may be used in the course of computation, by the use of the appropriate function number in the programme. In the middle is a group which simulates the ordinary instruction, and which is of great value in testing the machine without using a program, whilst the bottom row enables single digits in the main store to be changed. A prepulse switch initiates computations, which may proceed at 1,000 operations per second or at a reduced speed of 50 operations per second. Alternatively only one operation may be carried out for each movement of the key.

The right-hand panel has controls for the input-output equipment, high-tension "on" "off," and indicators showing the sign of the accumulator, multiplier, er cetera.

The cathode-ray tube display has along the top the contents of the four subsidiary stores, from right to left, the B-tube, control, accumulator, and multiplier tube. Underneath are the two main displays, each of which may be made to show the contents of any of the eight main stores. The input equipment consists of a specially developed photoelectric type of reader which can accept information at very high speed. As soon as the computer has called for a character from the input, the reader moves the tape on to the next character, and stops there until another input operation is called for. If the tape is stationary on a character, then the next character is available for reading in 5 milliseconds, giving a mean speed of 200

Figure 12. Details of valve and component failures



characters/second, whilst if the tape is not brought to rest, a maximum speed of 250 characters/second is possible. On test this equipment has read 500,000 characters at a time without error, and a loop of tape has been passed through the reader 10,000 times without any sign of wear. From experience to date this part of the equipment would appear to require maintenance at about three monthly intervals.

The output equipment is basically standard teleprinter apparatus, operating at normal teleprinter speeds. The most important addition to this equipment is a check system. Contacts are fitted to the interposers (for the punch) and combination combs (for the teleprinter) and the output operation is only released when these contacts have the same configuration as the electronic equipment operating the output system. Faulty operation of the contacts due to dirt et cetera, will result in a failure to check and computation will be stopped. Manual resets are provided to release the output equipment.

Present development work on the output equipment includes the provision of a tape punch operating at a speed of 50 characters per second, and a parallel type printer operating at 160 characters per second.

Applications of the Computer

The programmer will find that there are two points about this machine which differentiate it from most others—the presence of a large and readily available backing store, and the B tube. Of these two, the first is certainly the most important, as anyone who has coded for a machine with a restricted store will realize.

The provision of a magnetic storage drum has two effects from the point of view of the machine user. The first, of course, is that it widens considerably the class of problem which can be handled: for example, network analysis problems involving the inversion of symmetric matrices containing up to 80 × 80 complex elements are being tackled, and this task is still well within the capacity of the machine.

The other effect is perhaps not so obvious, but is even more important in the long run. The devices which a programmer must use in order to conserve space when he is operating with only a small store have perhaps only one thing to be said in their favor and that is that they give their inventors the feeling of satisfaction which usually arises from the solution of mathematical puzzles. Apart from this, such devices are usually error-provoking and they render programs containing them difficult to explain to the neophyte.

Once, then, the confining effect of a small store is removed, the justification for using 'tricks' becomes very much less, and a substantial saving in programming time results. This point can be best appreciated by those who have programmed for both a machine with small storage and one with which, for most problems, space virtually ceases be a consideration.

One other point about the use of a storage drum is that it becomes possible to keep many basic subroutines and machine testing routines permanently in the machine—a convenience which helps both the user and the maintenance engineer. In fact, the importance of some subroutines is such that the writing head associated with the track in which they occur is disconnected. They cannot then be written over by mischance.

The convenience of the B tube is greatest in routines which have a large number of varying addresses in the inner loop, matrix operations being typical—in such cases, program times may be more than halved. The B tube also is useful as a set of short-line accumulators for simple operations.

Subroutines

A fair basis of comparison between computing machines is the time taken to do various standard subroutines; a selection of these times follows. The times stated are the maximum times, and they include the time taken to transfer the subroutine from the storage drum to the cathode-ray tube store (0.03 seconds).

Square Roots and Reciprocal Square Roots

These are for convenience produced by one subroutine, the results being presented in standardized form. Time: 0.105 second.

Cosine

This forms the cosine of an angle between $-\pi$ and $+\pi$, and it is accurate to 11 decimal digits. Time: 0.08 second.

Natural Logarithm

This extracts the natural logarithm of a number lying between 2^{40} and 2^{-40}. Time: 0.08 second.

Reciprocal

The result is presented in standardized form. Time: 0.095 second.

Inverse Trigonometrical Routine

Given the sine and cosine of an angle, this finds the angle (lying between $+\pi$ and $-\pi$). Time: 0.10 second.

Reciprocal of a Matrix

Because of the organization of the transfer of information from the magnetic drum, matrix operations are most conveniently carried out by using 4 by 4 submatrices as the unit of operation. A reciprocating subroutine which standardizes each submatrix after operating on it is being developed, and it is expected that the approximate time taken to invert an $n \times n$ matrix will be $0.04\ n^3$ second.

Longer Calculations

Among the industrial computations which have been and are being carried out may be mentioned the following:

1. Investigation of the behavior of a cotton thread in a ring spinning device. This investigation now is complete and occupied in all ten hours of machine time (most of which was for actual computation). Taking into account centrifugal force and air resistance the problem involved the solution of a set of four linear simultaneous differential equations and was used as a test case for the general routine for solving such equations. The method used is one of the Runge-Kutta type giving 4th order accuracy in the length of the interval.

2. Computation of Laguerre functions. It is expected that about 30 hours of actual computing time will be taken up with the tabulation of the required functions, most of which will be printing time.

3. A study of power network problems requiring the computation of load flows and of machine swing curves. A program is being constructed which will have general application to any power network within the storage capacity of the machine.

Evaluation of Machine Performance to Date

For the purpose of this description the period July 14, 1951 to October 13, 1951 inclusive will be considered. The week beginning July 14, 1951 was the week following the formal handing over of the computer, and it has become apparent, even within these 13 weeks of operation, that several improvements can be made in the method of running a machine from an engineering view point.

When the system was first started, no formal maintenance period was allowed—the machine was switched on at 8:30 a.m. and handed over to the operators at 9 a.m. if working. Each operator was allocated a given number of hours per day, but if the machine became unservice-

able during an operator's period, then that operator was not recompensed for the time lost in servicing. Hence there was a tendency not to report faults, but to continue to attempt to use the machine.

This tendency was particularly noticeable when the faults were of an intermittent nature. After the first four weeks of operation this system was changed to one in which the allocation of time for a week was based upon the previous week's record. It is interesting to note the very large increase in fault time starting at the seventh week when the holiday period was over. Operators now are willing to devote time to helping the maintenance engineer trace faults always on the understanding that this time is booked as fault time.

As the system is worked at present, there is a fixed maintenance time—8:30 to 10:00 a.m.—each day, and the maintenance engineer is in attendance until 5:30 p.m. If the machine is serviceable at 5:30 p.m., it is kept in operation and is used until either the operators have completed their schedule of work or a fault develops. This system tends to cause violent fluctuations in nonmaintained operating time, as even a very simple fault will cause the machine to be closed down until the following day.

Nevertheless the long hours logged during nonmaintained hours are very encouraging and it is therefore the intention, as soon as maintenance engineers are trained, to put the machine on to a 24-hour service, probably for five days per week.

The time devoted to engineering covers a number of activities. Any computer can always be improved, especially in the first few months of its use for computation, and this machine has proved to be no exception. Part of the time shown in Figure 10 has been devoted to the installation of magnetic storage—only a very limited storage was available at the dedication date—a random number generator has been installed, and a number of circuit modifications made. As a result of the experience gained, new circuits are being developed, and these will be incorporated in the machine as they become available.

A total of 834 hours has been logged since dedication, with 74½ hours fault time, that is, practically 90 per cent availability. It is confidently expected that these figures will show a considerable improvement with better fault finding techniques and experience and longer periods of available maintenance.

A more detailed analysis of fault time, as shown in Figure 11, indicates that, as is to be expected, of the three subdivisions, the electronic equipment was responsible for the majority of faults—approximately 80 per cent of the total fault time. Most of the fault time in both the electronic equipment and the power supply equipment was due to valve failures, whilst mechanical faults caused most of the failure time in input-output equipment, due chiefly to the use of prototype equipment which was not suitable for prolonged operation. New input-output equipment is now installed with a consequent reduction of failures.

In the computer there are 4,000 valves, 12,000 resistors, and 2,500 condensers, and the total number of failures for each of the main valve types, and the components, is shown in Figure 12. It will be observed that there has been a total of 39 valve failures in the past 834 hours. If we assume an exponential valve life expectancy, we obtain an average valve life of 85,600 hours. In the same time there have been failures in three resistors and one condenser, which on the same basis leads to lives of 3,336,000 and 2,085,000 hours respectively. In view of the fact that standard, commercially available valves and components have been used, it is considered that these figures are satisfactory for what is still a running-in period.

Joint Discussion*

B. Moffat: (Mellon Institute): Dr. Kilburn, what speeding up, quantitatively, do you get through the use of the Williams' tube? In other words, at what speed does the arithmetic unit progress with respect to the relatively slow synchronized reading in the Williams' tube?

T. Kilburn: As I understand your question you mean what speed would you get if you left out the Williams' tube and just used the magnetic drum.

B. Moffat: No—as differentiated from the magnetic drum.

T. Kilburn: The digit frequency is 10 microseconds and the digit frequency on both the cathode-ray tube and drum is the same. The difference in speed is simply in the access times.

B. Moffat: I did not see why, if the drum and tube are synchronized, the access is faster with the Williams' tube.

T. Kilburn: The required line of the raster is immediately available. In the parallel machine the required spot area is immediately available.

W. L. Martin: (University of California, Los Angeles): A question of Mr. Pollard. I would like to ask the size of the cathode-ray tube and the approximate cost, also any data on the cost of the whole computer.

B. W. Pollard: The size of the cathode-ray tube is approximately 6 inches in diameter, and the tube is 14 or 16 inches long. The tube is made by the General Electric Company of Wembley, England. I do not think I am competent to quote the price they would quote to you—but it would be something of the order of £30.

Your second question was the price of a complete computer of the type we have been describing. We are proceeding with the construction of further models and we have at the present time two under construction, due to be completed in the next few months. One of those may be available at around $400,000 to $450,000, which will include free maintenance for one year, and also installation.

A. H. Taub (University of Illinois): I would like to ask either of the speakers about the organization of the various memories. If one has a problem such as a partial differential equation where the program is of the order of 3/4 of one of the pages and the initial data is of the same size, so at each stage if the solution one has to refer to a page and a half, does this mean that the machine is stopped or is there any other "out"?

T. Kilburn: There are eight cathode-ray tubes and—did you imply the total amount of data was just a page and a half?

A. H. Taub: I meant to imply that each step of the inner race cycle was, since there are eight cathode-ray tubes, 8½ pages.

T. Kilburn: I can assure you, on our machine that there are a lot of problems for which the cycle is less than eight cathode-ray tubes, because the choice of eight tubes is made on the basis that there are a lot of such problems. In the machine there are emergency compartments left for the provision of more cathode-ray tubes up to a maximum of 16.

J. Fedako (Eckert-Mauchly Computer Corporation): Did you mean to imply you can't print-out while computing?

B. W. Pollard: I merely meant that the Teleprinter is an awfully slow device at ten characters a second. However, in the output system, once the five digits have transferred to the output staticisers the machine is immediately released for further computation and the machine will only be stopped if another print-out order was called for, whilst the printing operation is going on. In other words, exactly the same system as the ERA 1101, which was described earlier this afternoon.

J. Brustman (Remington Rand): I have two questions. What is the dot and what is the dash time? Secondly, do you use any focusing or defocusing time and, also, do you use any automatic devices for holding, such as gain control, et cetera?

T. Kilburn: The defocus time is 1.8 microseconds and there is the "meditation" period of 1.2 microseconds whilst the computing circuit wonders what the answer is. There is then the focus time corresponding

* This joint discussion covers both this and the preceding paper by F. C. Williams and T. Kilburn on the University of Manchester Computing Machine.

to the dash period which is 4 microseconds followed by a blackout period, during movement to the next digit, a total of 10 microseconds. Speed of operation has not been a prime object of design. We have been content to accept the natural speed of operation of the components used in the machine and we have taken full advantage of the fact that we knew we were going to have a large storage capacity in the machine, giving quite a good speed of operation. Automatic control is applied only to the gain of the pick-up amplifier.

G. E. Reynolds (United States Air Force, Cambridge Research Center): I have a question for Dr. Kilburn. The random number generator that you mentioned—may we have a few details?

T. Kilburn: It operates on the principal that one takes a noise source and allows it to control a counter. The state of the counter is inspected every so often and the nought or one obtained is put in the accumulator of the machine and moved upwards before the next nought or one is put in. This continues until a 20-digit number is assembled in the accumulator.

E. Blumenthal (Eckert-Mauchly Computer Corporation): I would like to ask of either speaker the reason for using a servo system for the master oscillator to control the drums rather than the sprockets and using that as your oscillator.

T. Kilburn: This is an opening sentence in a debate that never ends, in England. I will tell you why we did that, and you can be the judge as to whether it is right or wrong.

In the early stages, we did not know whether or not we would have more than one drum inside the machine. If we did require this, then we should have had to synchronize the second drum to the first. Thus we faced this problem of locking in the drum to a master oscillator immediately. The servo-mechanism is extremely reliable.

The Whirlwind I Computer

R. R. EVERETT

PROJECT Whirlwind is a high-speed computer activity sponsored at the Digital Computer Laboratory, formerly a part of the Servomechanisms Laboratory, of the Massachusetts Institute of Technology (M.I.T.) by the Office of Naval Research (O.N.R.) and the United States Air Force. The project began in 1945 with the assignment of building a high-quality real-time aircraft simulator. Historically, the project has always been primarily interested in the fields of real-time simulation and control; but since about the beginning of 1947 most of its efforts have been devoted to the design and construction of the digital computer known as Whirlwind I (WWI). This computer has been in operation for about 1 year and an increasing proportion of project effort now is going into application studies.

Applications for digital computers are found in many branches of science, engineering, and business. Although any modern general-purpose digital computer can be applied to all these fields, a machine is generally designed to be most suited to some particular area. Whirlwind I was designed for use in control and simulation work such as air traffic control, industrial process control, and aircraft simulation. This does not mean that Whirlwind will not be used on applications other than control. About one-half the available computing time for the next year will be assigned to engineering and scientific calculation including research in such uses supported by the O.N.R. through the M.I.T. Committee on Machine Methods for Computation.

These control and simulation problems result in a specialized emphasis on computer design.

Short Register Length

WWI has 16 binary digits and the control problems are usually very simple mathematically. Furthermore, the computer is almost always part of a feedback rather than an open-ended system. Consequently, roundoff errors are seldom troublesome and the register length can be shortened to something comparable to the sensitivity of the physical quantities involved, perhaps five decimal places or less.

WWI has a register length of 16 binary digits including sign or about four and one-half decimals. The register length was chosen as the minimum that would provide a usable single-address order, in this case five binary digits for instruction and 11 binary digits for address. In a future machine we would probably increase this register length to 20 or 24 binary digits to get additional order flexibility; the increased numerical precision is less important.

For scientific and engineering calculation, greater than 16-digit precision is often required. There is available a set of multiple-length and floating point subroutines which make the use of greater precision very easy. It is true that these subroutines are slow, bringing effective machine speed down to about that obtained by acoustic memory machines. It is much more efficient occasionally to waste computing time this way than continuously to waste a large part of the storage and computing equipment of the machine by providing an unnecessarily long register.

High Operating Speed

WWI performs 20,000 single-address operations per second. Control and simulation problems require very high speeds. The necessary calculations must be carried out in real time; the more complex the controlled system is, the faster the computer must be. There is no practical upper limit to the computing speed that could be used if available.

Where the problems are large enough, and these problems are, one high-speed machine is much better than two simpler machines of half the speed. Communication between machines presents many of the same problems that communication between human beings presents.

Great effort was put into WWI to obtain high speed. The target speed was 50,000 single-address operations per second, and all parts of the machine except storage meet this requirement. The actual WWI present operating speed of 20,000 single-address operations per second is on the lower edge of the desired speed range.

Large Internal Storage

WWI now has 1,280 registers. A large amount of high-speed internal storage is needed since it is not in general possible to use slow auxiliary storage because of

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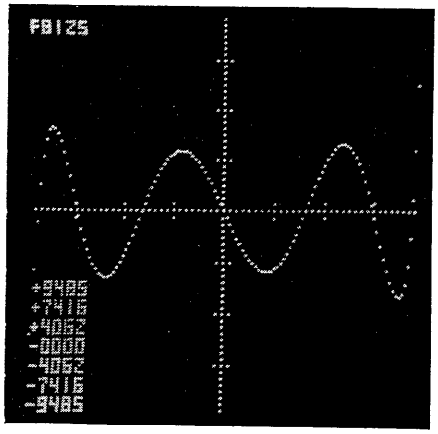


Figure 1. Sample computer output

the time factor. In many cases a magnetic drum can be useful since its access time is short compared to the response times of real systems. Even with a drum there is considerable loss of computing and programming efficiency due to shuffling information back and forth between drum and computer.

WWI is designed for 2,048 registers of storage. Until recently there has been available only about 300 registers. This number, while small, has been adequate for much useful work. Very recently a second bank of new-model storage tubes has been added. These new tubes operate at 1,024 spots per tube bringing the total WWI storage to 1,280 registers. These tubes have been in the computer and under test for 2 months and in active use for about 2 weeks. In the next few months the tubes in the first bank will be replaced by new model storage tubes bringing the total storage to 2,048. This number is on the lower end of what the project considers desirable. What the computer business needs, has needed, and will probably always need is a bigger, better, and faster storage device.

Extreme Reliability

In a system where much valuable property and perhaps many human lives are dependent on the proper operation of the computing equipment, failures must be very rare. Furthermore, checking alone, however complete, is inadequate. It is not enough merely to know that the equipment has made an error. It is very unlikely that a man, presumably not too well suited to the work during normal conditions, can handle the situation in an emergency. Multiple machines with majority rule seem to be the best answer. Self-correcting machines are a possibility but appear to be too complicated to compete, especially as they provide no standby protection.

The characteristics of the Whirlwind I computer may be recapitulated as follows:

Register length	16 binary digits, parallel
Speed	20,000 single-address operations per second
Storage capacity	Originally 256 registers Recently 320 registers Presently 1,280 registers Target 2048 registers
Order type	Single-address, one order per word
Numbers	Fixed point, 9's complement
Basic pulse repetition frequency	1 megacycle 2 megacycles, (Arithmetic element only)
Tube count	5,000, mostly single pentodes
Crystal count	11,000

There are 32 possible operations, of which about 27 are assigned. They are of the usual types; addition, subtraction, multiplication, division, shifting by an arbitrary number of columns, transfer of all or parts of words, subprogram, and conditional subprogram. There are terminal equipment control orders and there are some special orders for facilitating double-length and floating-point operations.

One way to increase the effective speed of a machine is to provide built-in facilities for operations that occur frequently in the problems of interest. An example is an automatic co-ordinate transformation order. The addition of such facilities does not affect the general-purpose nature of the machine. The machine retains its old flexibility but becomes faster and more suited to a certain class of problems.

From March 14, 1951, at which time we began to keep detailed records, until November 22, 1951 a total of 950 hours of computer time were scheduled for applications use. The machine has been running on two shifts or a total of about 3,000 hours during this interval. The two-thirds time not used for applications has been used for machine improvement, adding equipment, and preventive maintenance.

Of the 950 hours available, 500 have been used by the scientific and engineering calculation group, the rest for control studies. The limited storage available until recently has been admittedly a serious handicap to the scientific and engineering applications people. There has not been room in storage for the lengthy subroutines necessary for convenient use of the machine. The largest part of their time has been spent in training, in setting up procedures, and in preparing a library of subroutines.

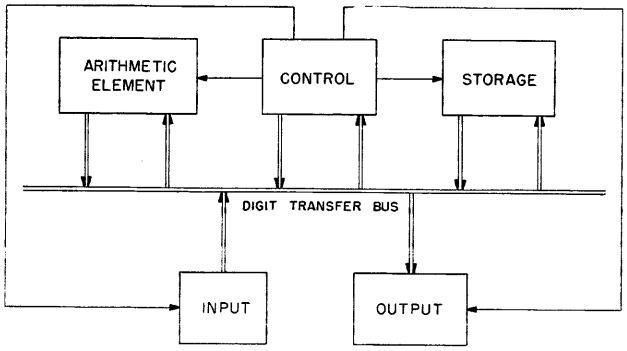
A partial list of the actual problems carried out by the group includes:

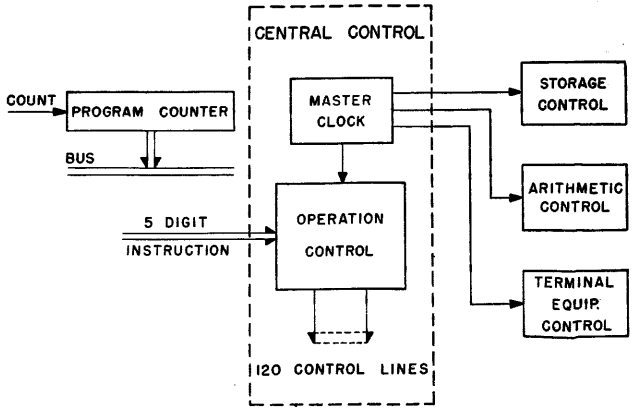
1. An industrial production problem for the Harvard Economics School.
2. Magnetic flux density study for our magnetic storage work.
3. Oil reservoir depletion studies.
4. Ultra-high frequency television channel allocation investigation for Dumont.
5. Optical constants of thin metal films.
6. Computation of autocorrelation coefficients.
7. Tape generation for a digitally-controlled milling machine.

The scientific and engineering applications time on Whirlwind I has been organized in a manner patterned after that originated by Dr. Wilkes at EDSAC. The group of programmers and mathematicians assigned to WWI assist users in setting up their own problems. Small problems requiring only a few seconds or

Figure 2 (below). Simplified computer block diagram

Figure 3 (right). Control





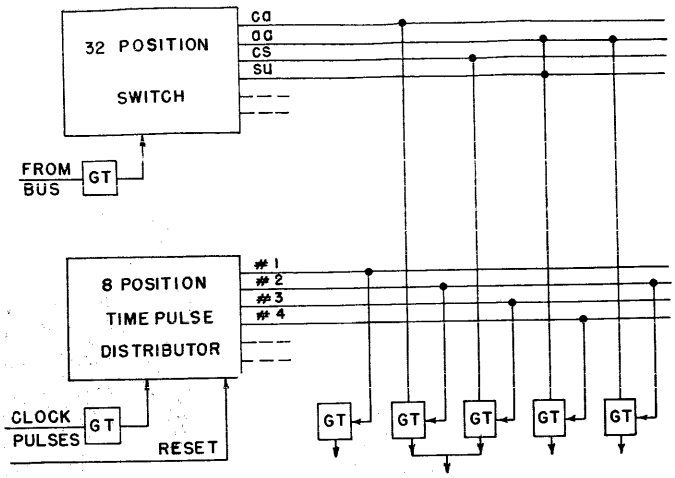


Figure 4. Operation control

minutes of computer time are encouraged. Applications time is assigned in 1-hour pieces two or three times a day. No program debugging is allowed on the machine. Program errors are deduced by the programmer from printed lists of results, storage contents, or order sequences as previously requested from the machine operator. The programmer then corrects his program which is rerun for him within a day or perhaps within a few hours.

Every effort is made to reduce the time-consuming job of printing tabulated results. In many cases a user desires large amounts of tabulated data only because he doesn't really know what answers he wants and so asks for everything. Such users are encouraged to ask only for pertinent results in the form of numbers or curves plotted by the machine on a cathode-ray tube and automatically photographed. If these results prove inadequate or the user gets a better idea of his needs, he is allowed to rerun his program, again asking only for what appear to be significant results. Figure 1 shows a sample curve plotted by the computing machine showing calibrated axes and decimal intercepts.

WWI System Layout

Figure 2 shows the major parts of any computer such as WWI. The major elements of the computer communicate with each other via a central bus system.

WWI is basically a simple, straightforward, standard machine of the all-parallel type. Unfortunately, the simple concept often becomes complicated in execution, and this is true here. WW's control has been complicated by the decision to keep it completely flexible; the arithmetic element by the need for high speed, the storage by the use of electrostatic storage tubes, the terminal equipment by the diversity of input and output media needed.

Control

The WW control is divided into several parts, as shown in Figure 3.

Central Control

The central control of the machine is the master source of control pulses. When necessary the central control allows one of the other controls to function. In general there is no overlapping of control operation; except for terminal equipment control, only one of the controls is in operation at any one time.

Storage Control

Storage control generates the sequence of pulses and gates that operate the storage tubes. Central control instructs the storage control either to read or to write.

Arithmetic Control

Arithmetic control carries out the details of the more complex arithmetic operations such as multiplication and division. The setup of these operations plus the

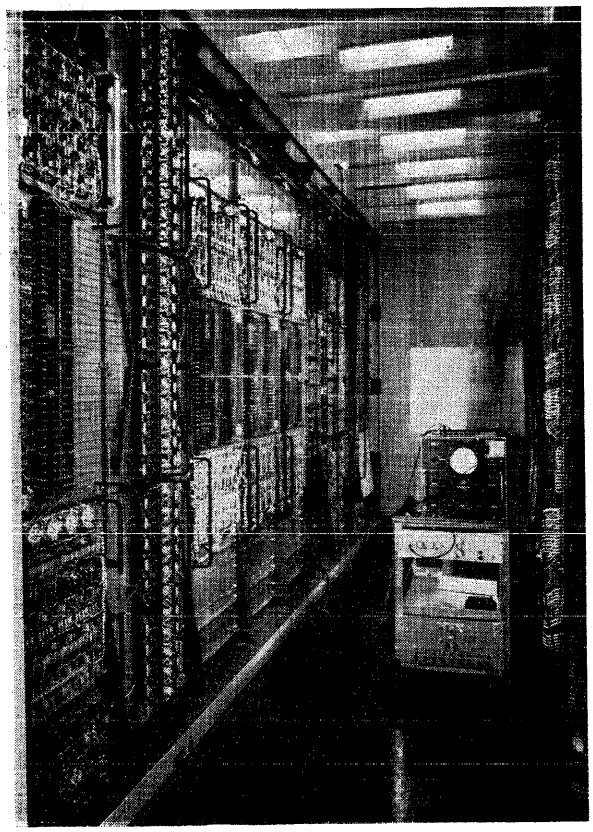


Figure 5 (left). View of central control

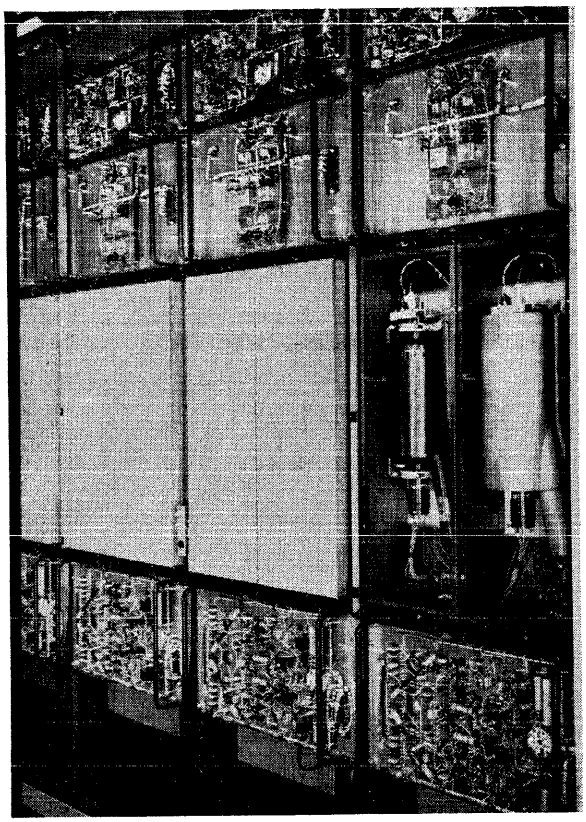


Figure 6 (right). View of electrostatic storage

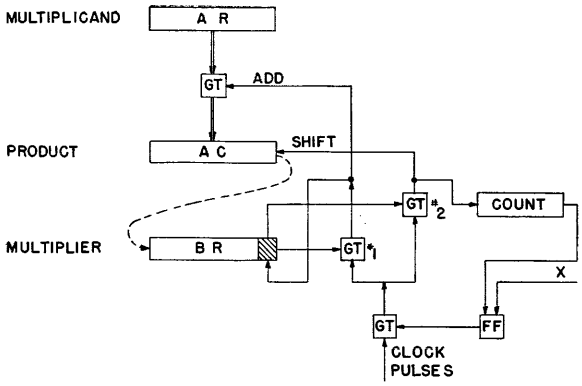


Figure 7 (above). Arithmetic element

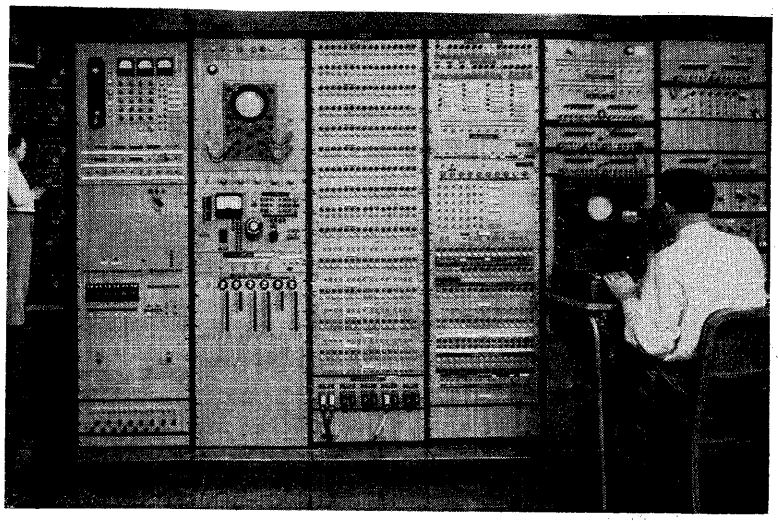


Figure 9 (right). View of test control

complete controlling of the simpler operations such as addition are carried out by central control.

Terminal Equipment Control

Terminal equipment control generates the necessary control pulses, delay times, and interlocks for the various terminal equipment units.

Program Counter

The program counter which keeps track of the address of the next order to be carried out is considered as part of control. This is an 11-stage binary counter with provision for reading to the bus.

Most of the functions of these subsidiary controls could be combined with the central control. The major reason they are not is that they were designed at different times. The arithmetic element and its control came first, followed by central control. At the time central control was designed, the necessary characteristics of storage control were unknown. In fact, the machine was designed so that any parallel high-speed storage could be used. The form of terminal equipment control was also unknown at this time. Since flexibility was a prime specification, it was felt preferable to build separate flexible controls for the various parts of the computer than to try to combine all the needed flexibility in one central control.

In a new machine we would attempt to combine control functions where possible, hoping to have enough prior knowledge about component needs to eliminate subsidiary controls completely. We would still insist on a large degree of control flexibility.

Master Clock

The master clock consists of an oscillator, pulse shaper and divider that generate 1- and 2-megacycle clock pulses, and a clock pulse control that distributes these clock pulses to the various controls in the machine. It is this unit that determines which of the subsidiary controls actually is controlling the machine. This unit also stops and starts the machine and provides for push-button operation.

Operation Control

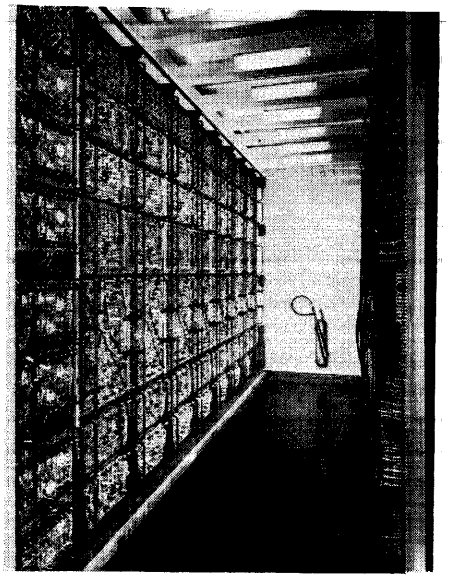
The operation control, see Figure 4, was designed for maximum flexibility and minimum number of operation digits, and, consequently, minimum register length. It is of the completely decoding type.

The operation switch is a 32-position crystal matrix switch that receives the 5-bit instruction from the bus and in turn selects one of 32 output lines corresponding to the 32 built-in operations.

There are 120 gate tubes on the output of the operation control. Pulses on the 120 output lines go to the gate drivers, pulse drivers, and control flip-flops all over the machine; 120 is a generous number. The suppressors of these gate tubes are connected to vertical wires that cross the 32 output lines from the operation switch. Crystals are inserted at the desired junctions to turn on those gate tubes that are to be used for any operation.

The time pulse distributor consists of an 8-position switch driven from a three binary-digit counter. Clock pulses at the input are distributed in sequence on the eight output lines. The control grids of the output gate tubes are connected to these timing lines. The output of the operation control is thus 120 control lines on each of which can appear a sequence of pulses for any combination of orders at any combination of times.

Figure 8. View of arithmetic element



Central Control

The Central Control of the machine is shown in Figure 5. The control switch is in the foreground with the operation matrix to the right.

Electrostatic Storage

The electrostatic storage shown in Figure 6 consists of two banks of 16 storage tubes each. There is a pair of 32-position decoders set up by address digits read in from the bus. There is a storage control that generates the sequence of pulses needed to operate the gate generators, et cetera. A radio frequency pulser generates a high power 10-megacycle pulse for readout.

Each digit column contains, besides the storage tubes, write plus and write minus gate generators and a signal plate gate generator for each tube. Ten-megacycle grid pulses are used for readout in order to get the required discrimination between the fractional volt readout pulses and the 100-volt signal plate gates. For each storage tube there is a 10-megacycle amplifier, phase-sensitive detector and gate

tube, feeding into the program register. The program register is used for communicating with the storage tubes. Information read out of the tubes appears in the program register. Information to be written into the tubes must be placed in the program register.

Arithmetic Element

The arithmetic element, see Figure 7, consists of three registers, a counter, and a control.

The first register is an accumulator (AC) which actually consists of a partial-sum or adding register and a carry register. The accumulator holds the product during multiplication.

The second or A-register holds the multiplicand during multiplication. All numbers entering the arithmetic element do so through AR.

The third or B-register holds the multiplier during multiplication. The accumulator and B-register shift right or left. A high-speed carry is provided for addition. Subtraction is by 9's complement and end-around-carry. Multiplication is by successive additions, division by successive subtractions, and shift orders provide for shifting right or left by an arbitrary number of steps, with or without roundoff.

The arithmetic element is straightforward except for a few special orders and the high speed at which it operates. Addition takes 3 microseconds complete with carry; multiplication, 16 microseconds average including sign correction.

In figure 8 are shown several digits of the arithmetic element. The large panels are accumulator digits. Above the accumulator is the B-register below it the A-register.

Test Control

Test control, shown in Figure 9, is used at present both for operating and for trouble shooting the computer. The control includes:

1. Power supply control and meters.
2. Neon indicators for all flip-flops in the machine.
3. Switches for setting up special conditions.
4. Manual intervention switches.
5. Oscilloscopes for viewing wave forms. A probe and amplifier system allows viewing any wave form in the computer on one scope at test control.
6. Test equipment to provide synchronizing, stop, or delay pulses at any step of any order of a program, allowing viewing wave forms on the fly anywhere in the machine.

An important part of the test facilities is the test storage, a group of 32 toggle-switch registers plus five flip-flop registers that can be inserted in place of any five of the toggle-switch registers. This storage has proved invaluable not only for testing control and arithmetic element before electrostatic storage was available but also for testing electrostatic storage itself. When not in use for test purposes test storage earns its keep as part of the terminal equipment system. The toggle-switches hold a standard read-in program; the flip-flop registers are used as in-out registers for special purposes.

Checking

Logical checking facilities built into WWI are rather inconsistent. A complete bus transfer checking system has been provided, duplicate checking of some terminal equipment is permitted, but little else is thoroughly checked. We felt that it was worth while to thoroughly check some substantial portion of the machine. This portion would then serve as a prototype for studying the tube circuitry used throughout the machine. We did not feel it was worth while to check all the machine, a procedure that requires a great deal of added equipment and logical complexity plus a substantial loss in computing speed.

Operating experience has shown us that it is not worth while to provide detailed logical checking of a machine. In a new machine we would leave out the transfer checking. The amount of information and security given by the detailed checking system is not enough to warrant the expense of building and maintaining it.

This decision is based on the expectation that a computing machine should operate 95 per cent of total time or better and that the average time between random failures should be of the order of 5 to 10 hours or approximately 10^9 operations.

In our opinion the way to achieve the extremely high reliability needed in some real-time control problems is to provide three or more identical but distinct machines, thus obtaining error correction as well as detection, plus such features as standby, safety, and damage control. Even so the failure probability of each machine must be kept low by proper design, marginal checking, and preventive maintenance.

Extremely high reliability means a reliability far beyond that achieved in existing machines and not conveniently represented as a per cent. Consider a system consisting of three machines, each operable 98 per cent of the time and each averaging 10 hours between random errors.

One machine will be out of operation 1/2 hour per day.

Two machines will be out of operation 1/4 hour per month.

All three machines will be out of operation 4 minutes per year. Furthermore undetected random errors might occur on the average of once a year. Such reliability is needed in some systems.

Our decision to omit detailed checking does not extend to checking devices intended to detect programming errors. Devices to check for overflow from the arithmetic element or for nonexistent order configurations are necessary. Programmers make many mistakes. Techniques for dealing with programming errors are very important and need future development.

Terminal Equipment

At the present time, Whirlwind is using the following terminal equipment:

1. A photoelectric paper tape reader.
2. Mechanical paper tape readers and punches.
3. Mechanical typewriters.
4. Oscilloscope displays 5 to 16 inches in diameter with phosphors of various persistencies including a computer-controlled scope camera.
5. Inputs from various analogue equipments needed for control studies.
6. Outputs to analogue equipment.

To be added during the next year:

1. Magnetic Tape (units by Raytheon). One such unit is now being integrated with machine.
2. Magnetic drums (units by Engineering Research Associates, Inc.).
3. Many more analogue inputs and outputs.

This great complexity of terminal equipment requires a flexible switching system. There is a single in-out register (IOR) through which most of the data passes.

There is a switch which is set up by an order to select the desired piece of terminal equipment. Other orders put data into IOR or remove data from IOR. The in-out control provides the necessary control pulses to go with each type of equipment. In general the computer continues to run during terminal equipment wait times; suitable interlocks are provided to prevent trouble. This complete equipment has not yet been fully installed.

(Discussion of this paper was combined with that of the following paper)

Evaluation of the Engineering Aspects of Whirlwind I

NORMAN H. TAYLOR

THE Whirlwind system is an expanding one now adding terminal equipment such as magnetic tapes, drums, and scopes. The core of the system including control, memory, and arithmetic element now has been running long enough to make an engineering evaluation of its performance, so the following comments will apply mainly to these three sections.

Measured in terms of applications performance, Whirlwind has been used about 950 hours in the last 6 months, but the basic elements have accumulated over 8,000 hours of use during engineering tests over the last year and a half.

A current running day in the Whirlwind system has 5 to 8 hours assigned to application engineering, 6 hours to engineering development such as the extension of terminal facilities and the increase in the internal storage capacity, and 1 hour to marginal checking.

To express the performance record during the applications period, we have taken a ratio of the total number of productive hours to the total assigned hours and get a figure of 85 per cent as our over-all efficiency. A more detailed study of the remaining 15 per cent of time indicates that the people using the machine are responsible for about two-thirds of this down time while the machine itself is responsible for about one-third. This is due to the fact that the machine schedules are made 1 week in advance and if an engineering test takes an hour longer than the schedule indicates, this is counted as down time. Omitting these scheduling problems, machine efficiency is close to 95 per cent.

Another way of evaluating the system is to look at the number of replacements of components in a period of time. Whirlwind now contains 4,450 tubes, most of which have been in their sockets about 8,000 hours. Of these, 616 have been removed for a total of 14 per cent tube removal. This gives a failure rate of 1.7 per cent per 1,000 hours.

Whirlwind contains about 11,000 crystals in two rather widely separate applications. A large group of crystals, over 9,000, are used in low forward current and low back voltage applications and the performance record has been quite satisfactory. Only 180 replacements have been necessary in 8,000 hours for a total of 2 per cent. Expressed in the failure rate per 1,000 hours this number is 0.25 per cent.

A smaller group of 1,048 crystals has been used in clamping circuits at rated back voltage but much poorer results were attained, and 334 units or 31 per cent of these crystals have been removed for a rate of 4 per cent per 1,000 hours.

Before looking into the details of just where these failures arose, it may be well to say that the nature of a failure is very often more important than the fact that a failure exists; for instance: the marginal checking procedure which is an integral part of the Whirlwind system, makes it very easy for one to locate a slowly deteriorating component before it causes a systems failure, and replacement of such a component during a period of marginal checking or preventive maintenance does not hinder the user of the computer. A sudden failure, however, due to an intermittent joint can usually not be predicted. Such failures are apt to occur during an important calculation and breakdown at this time can be very expensive and time consuming. Over half of the failures in the Whirlwind system are now being picked up during the marginal checking period and these do not represent a major obstacle to its use in application periods. The effectiveness of this marginal checking lies somewhere between 50 and 70 per cent of the total failures which do occur. Our experience indicates that one may expect 6 to 10 hours of trouble-free operation after each marginal checking period. On the average, three tubes or crystals are replaced during the daily preventive maintenance period, but a breakdown of the system during an applications period only occurs about once in a 3-day period.

Breakdown of Performance Numbers

The numbers just quoted represent over-all systems performance. To discuss which portions are good and which are inferior from an engineering point of view, the system has been separated into sections as follows:

1. The flip-flop and gate used in arithmetic circuits and portions of control.
2. The control selection system.
3. The memory system (electrostatic storage tube circuitry).
4. Terminal equipment.

To evaluate each of these sections of Whirlwind, a look at the replacement rate of components is enlightening. This rate is to be based on replacements of vacuum tubes and germanium diodes because troubles can usually be traced to failure of one of these two components. Transformers, condensers, delay lines, and resistors are considerably better than tubes or crystals and may be considered quite adequate for use in computers of the future.

First, the gate circuit: A coincident *and* gate is made up of a *7AK7* gate tube, a transformer, and diode as shown in Figure 1. The grids are usually held at −15 volts, and a 20-volt pulse 0.1 microsecond wide is applied to grid number one. When the gate is sensed in this way, if grid 3 is at −15 volts no plate current flows; if grid 3 is at ground, about 30 milliamperes of plate current flows and a 0.1 microsecond pulse passes to the next circuit.

There are 1,300 gate circuits such as this in Whirlwind I (WWI), and the over-all failure rate of these circuits is the very best in the system. It is less than 0.5 per cent per 1,000 hours. The rate of failure seems to be linear, so if we dare to extrapolate, this slope indicates that half of our gate tubes will still be in use at 100,000 hours. Almost all the failures in this circuit are intermittent or mechanical in nature. Improvement in performance would undoubtedly demand considerable improvement in the method of production of vacuum tubes with special attention to cathode flaking, grid spacing, welding, and vacuum techniques.

The excellent performance of this circuit is due, of course, to the availability of the *7AK7* gate tube and its rather ideal application. This tube was designed and built for WW by Sylvania Electric Products, Inc. It is made in a pilot plant with special attention paid to cleanliness, uniformity of parts, vacuum pumping, aging, and choice of cathode materials. Our experience with other tubes indicates that the removal of this tube from the pilot plant production could easily reduce its performance to the level of other tubes.

The flip-flop circuit is a second basic element in the Whirlwind system and is

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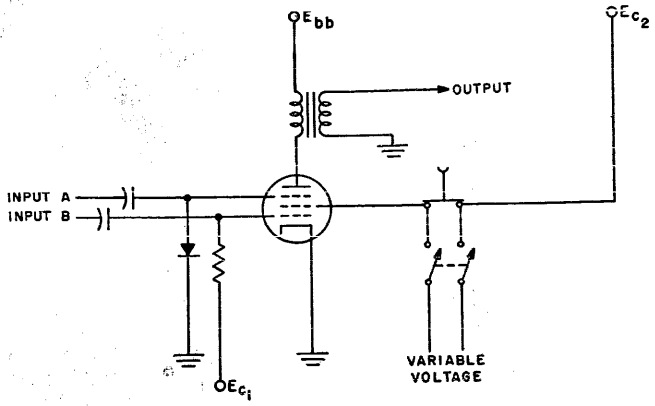


Figure 1. Marginal checking of gate circuit

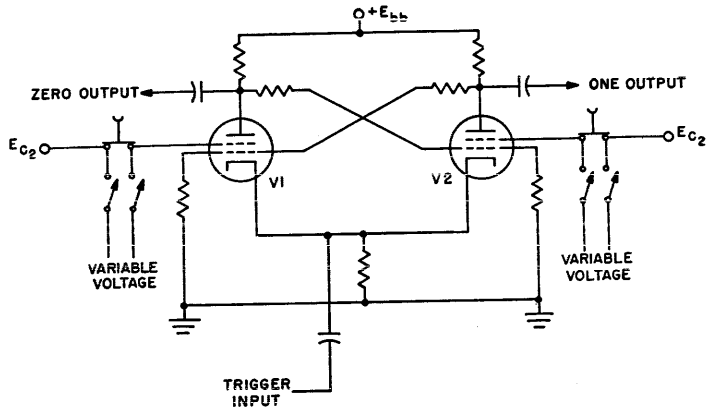


Figure 2. Original whirlwind flip-flop

used in many control and arithmetic portions of the system. Figure 2 is a schematic of the early version of the Whirlwind flip-flop. The high-speed switching requires flip-flop reversals in 0.2 of a microsecond or less. This sort of speed requires low impedance in a flip-flop circuit and the resultant d-c drain is high. That is, the cross-over arms in this original high-speed flip-flop draw so much current that the off tube has a considerable drop in its plate resistor. This fact makes direct coupling to gate circuits a problem requiring well-regulated supplies. To avoid this, the original Whirlwind circuitry used a-c coupling from flip-flops to gate circuits with restorer pulses and clamp crystals associated with each flip-flop. Two facts become evident after a few thousand hours:

1. Restorers are very time consuming and complicate the timing and control
2. Clamp crystals in high-speed circuits are poorly used and have a very high failure rate.

The replacement rate of tubes on the older type circuit has been rather high, 6.5 per cent per 1,000 hours. Clamp crystals were replaced at a rate of 4 per cent per 1,000 hours and this original circuit was definitely a weak point in the original WW system.

The marginal checking schedule of Whirlwind, however, allows the inferior circuitry originally employed to function rather effectively. Both tube and crystal failures which plagued these circuits were of a slow, deteriorating nature, and injection of marginal voltages on the screens as shown in the figure allow the removal of tubes or crystals well before they approached the dangerous error-generating condition.

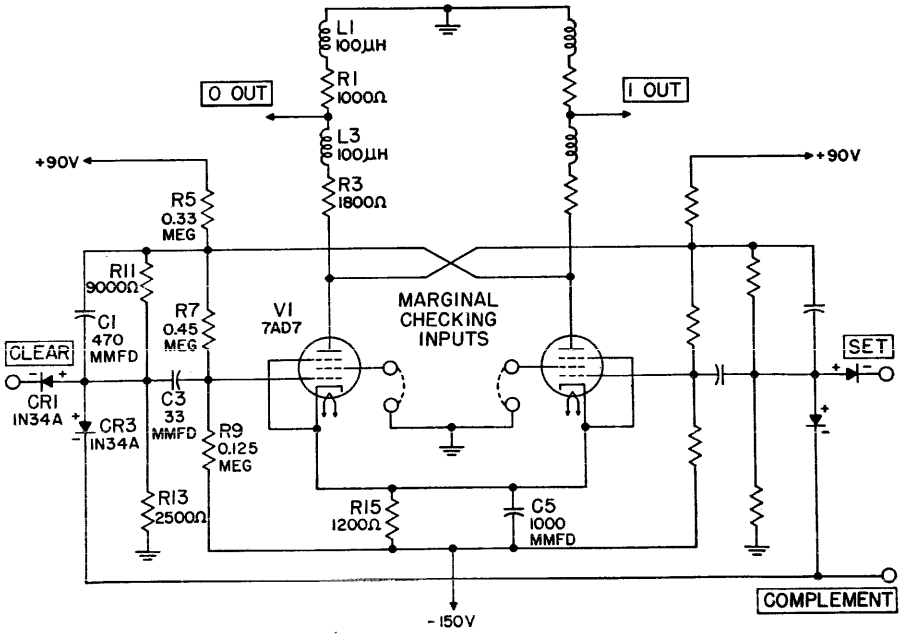
The revised circuit of Figure 3 eliminates these objections by a double voltage divider as shown on the drawing. The low impedance divider draws no d-c through the load resistor in the off condition. The high impedance divider draws such a small amount of current through the load resistor that it can be bucked out by a high impedance bleeder *R5* and *R6* connected to a 90-volt supply. This sends a current through *R1* and *R2* in the reverse direction. During switching the low-impedance divider follows the low-plate resistor rapidly and the large condenser between the junction of *R11* and *R13* to the junction point *R7* and *R9* does not allow the high impedance circuit to lag behind during the switching period. The split load *R1* and *R3* allows the tubes to operate more conservatively with no loss in speed and true cathode follower action can be attained by eliminating grid current in the on tube. Tubes can age in this circuit to a much lower value than in the original circuit without getting to a point of marginal operation.

There are 310 flip-flops in WWI. To date, the failure rate in these circuits has been about 10 per cent per 1,000 hours, 20 times poorer than the gate circuit. The revised circuit will give some improvement in this regard but data is not yet available. One can safely say that flip-flops are not the best type of circuits for high-speed computers, but it is not clear just what should be used to replace this element.

Control Circuitry

The central control of Whirlwind is arranged in the form of two crystal matrices, shown in Figure 4. One is a 32-position control switch to decode the order selection and the second an operation control matrix where one horizontal selection makes a large number of vertical selections. The capacitance of this array is such that rather large driving tubes are used as buffers both between the flip-flops and the matrix and along the selected line. Once a given set of channels is selected, the pulses carrying out the operation must be amplified to drive a

Figure 3. Flip-flop d-c coupled to its load



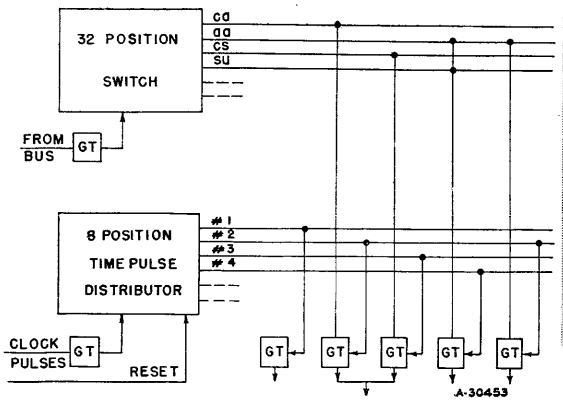


Figure 4. Operation control

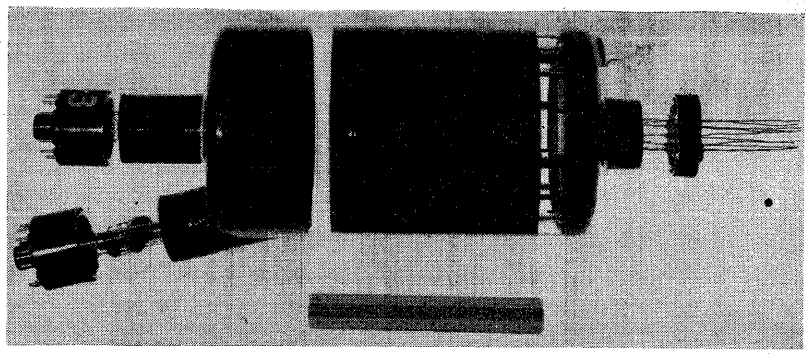


Figure 5. MIT storage tube

parallel register of 16 digits or read out to a central bus system for distribution or transfer.

This over-all control system contains 1,200 tubes and 2,700 crystals. The over-all failure rate is about 2 per cent per 1,000 hours and is due almost entirely to tube failures. Crystal failures are less than 0.06 per cent per 1,000 hours in this circuitry.

A detailed study of tube replacements here indicates that the larger buffer tubes are removed more often than the other types. This general approach to the control problem seems to be very satisfactory in a pulse system and an improved circuit in the power amplifiers would improve the replacement rate considerably. Of more significance are the excellent results obtained in the crystal matrices. These circuits were designed to tolerate back resistance values of as low as 10,000 ohms in the crystals—only one-tenth of rating. There is no doubt that this is a significant factor in their low replacement rate.

Memory

Whirlwind uses the MIT electrostatic storage tube as its high-speed internal memory. This tube has been developed, constructed, and is being produced by the Digital Computer Laboratory. Figure 5 is a photograph of the tube. The double neck houses two electron guns. This is not a Williams storage tube. It differs in the following ways:

Instead of regeneration of charge in a cyclic manner, a second gun is placed in the tube envelope. This is called a holding gun. It floods the storage area with low velocity electrons which replace any leakage of charge which occurs to produce a storage which is permanent as long as the holding gun remains turned on. This is made possible by the secondary emission properties of a special beryllium storage plate placed in the end of the tube.

Storage does not depend on a change in the geometry of the spot but rather a change in potential.

The 2,000-volt high-velocity gun is used to either read or write but during reading a 10-megacycle carrier is used and this makes the readout amplifier capable of distinguishing between the signal pulse and the switching transients.

The tube has a 10-microsecond access for reading and a 30-microsecond access for writing.

The data on just how well this portion of the system performs is colored by constant engineering improvements and design changes, and to take the number of hours, divided by the replacements as a measure of reliability, would be misleading. We can say that during the last 6 months over-all systems performance is not limited by lack of storage reliability any more than other portions of the system. However, the rather satisfactory use factor does depend on marginal checking.

The actual life of the storage tubes in the system and cause of failure can be summarized as follows:

From March to October (1951) the total tubes replaced in 16 sockets were 14. A total of 2,500 hours of operation during this period gave an average tube life of 1730 hours.

Quantity	Replacement of Storage Tubes
3	High velocity gun deterioration
7	Ion bombardment of storage surface
2	Nonuniform spot size
2	Miscellaneous reasons

The failures have been due to two main causes: first, deterioration of the writing gun below usable current levels; and second, contamination of the storage surface due to a positive ion bombardment.

Design changes are being incorporated to minimize these two factors as major reasons for short storage tube life. Considerable progress has been made.

Associated Memory Circuitry

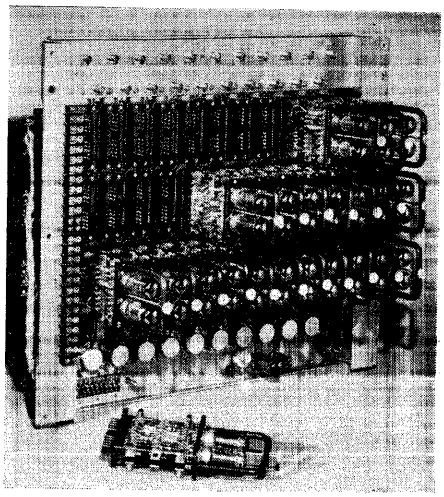
The over-all performance of the memory depends on a lot of circuitry including gate generators, reading amplifiers, deflection circuits and control. This system includes about 1,400 tubes and 1,400 crystal diodes and shows a failure rate of 3 per cent per 1,000 hours. The numbers quoted do not allow for slow changes or drifts which occur and must be corrected during the marginal checking preventative maintenance period.

In particular, adjustment of the writing gates and the focus voltage makes use of the marginal checking equipment. This adjustment accounts for slow changes in storage tube characteristics. The time element to adjust the operating point of tubes in the memory has been reduced to a few hours a week. This cannot be overlooked as a major factor in establishing the rather high use factor in Whirlwind.

Deflection

The deflection system associated with the storage is one of the most exacting portions of the Whirlwind Computer. In fact, this portion of the system is a digital to analogue converter with difficult requirements of power and speed. The

Figure 6. Plug-in unit assembly



converter must take binary numbers representing an address in the memory and convert these numbers to analogue voltages in the X and Y planes. These voltages must be amplified and transmitted to 32 storage tubes to deflect the high-velocity beam to the particular area to be used. This deflection process is carried out in about 0.5 microsecond but must be d-c coupled so that holding can occur for a long period.

It is important that high reproducibility in deflection be attained. Linearity is not a difficult requirement, but the precision must be about 0.25 per cent for short as well as long periods. This problem has been one of design and elimination of spurious effects. The system contains about 100 tubes and 60 crystals and the replacement rate is quite high, about 15 per cent per 1,000 hours. It cannot be said that this is a really desirable feature of Whirlwind and a better approach to the selection problem is needed.

Summary of Storage System

In summary the electrostatic storage system as used in Whirlwind works adequately. By making adjustments to the voltage gates which run the tubes on a weekly basis, it is possible to obtain reliable memory about 90 to 95 per cent of the time for periods as long as 50 hours. Storage tube life is still a problem and considerable preventative maintenance is definitely assumed as part of such a system.

We are very proud of the 1,024 spot storage tube now installed in the system. Early tests indicate comparable performance with the 256 bit tube, and although it is still too early to evaluate this 1,024 bit storage tube, several successful computer programs have already been run using the new bank of 16 tubes as a memory.

Terminal Facilities

WWI now operates with a photoelectric reader with punched paper tape for its input medium. The photo reader works well with opaque paper but is quite marginal if the usual yellow semitransparent tapes are used. The standard Flexowriter reader is also available.

The data on survival of components is not too significant on this terminal equipment. Failures are often due to dirty contacts in the relays or drifting currents in the circuits. A really good maintenance schedule seems to be the best solution to the terminal equipment problem.

Mechanical Design

The new installations of Whirlwind will follow a more compact mechanical pattern than the early bread board type of design. Figure 6 shows the new decoder housing 33 plug-in units. Seven square feet of panel space is used compared to the 46 square feet necessary for the original type of Whirlwind construction. The sockets are mounted on 0.5-inch square aluminum bars. Both power and signal wiring is made in the rear on open wires. This compact arrangement has not been made at the expense of reliability or circuit performance. It is really repackaging, not miniaturization. Of course, more cooling will be needed in this compact type of construction.

At the bottom of the picture a single high-speed flip-flop with the new type circuit is shown. Two other circuits have been packaged this way, the standard gating circuit and the switch tube for the decoder.

Conclusions

In closing it may be well to emphasize the strong and weak points of the Whirlwind system:

Good Points

1. The parallel short-register high-speed system is well adapted to real time control problems. The 16-digit register is rather short but 24 digits may well be quite sufficient.

2. Single address orders seem best when a high-speed memory is available.

3. Certain circuits such as the Whirlwind gate circuit show such excellent life that they deserve consideration for future machines.

4. Crystal matrices for control selection have excellent life-reliability characteristics.

5. Marginal checking is a definite must to keep large systems working a high percentage of the time.

Adequate Points

1. Electrostatic storage does work when adequate marginal checking is employed. The analogue deflection, cathode deterioration of guns and storage surface problems are not entirely solved.

2. Flip-flops are not entirely free of tube deterioration problems and reliable service depends on marginal checking.

Doubtful Points

1. The use of restoration to avoid d-c coupling is undesirable.

2. The use of clamp circuits using crystals in high-speed circuits is not good engineering design.

3. Coax coupling between circuits at pulse frequencies of 1 or 2 megacycles is costly and unnecessary.

Joint Discussion*

W. A. Farrand (North American Aviation, Inc.): Besides screen voltage variation, what marginal checking procedures do you use?

N. H. Taylor: Screen voltage variation seems to be about the nicest variable when you are using pentode tubes. If you do not have pentode tubes you put the variation on plates of triodes. We are beginning to use new techniques in the storage tube system. If you are charging the surface of a dielectric and want to find out the condition of the cathode, you may check whether it charges the dielectric in a fixed amount of time. This will give you an idea as to the condition of the high velocity writing gun, by marginal checking the time needed to charge to a given potential. We use pulse-repetition frequency to some extent, to check the discharge time of a crystal condenser circuit.

We are using a voltage increment in a deflection system to find out whether our reading and writing beam tracks are registering properly, in a little different way than just the usual system. I think almost anything you measure you can automatize and use as a means of marginal checking.

W. J. Wachter (Moore School of Electrical Engineering): You mentioned a 5-minute time for slow turn-on. What does this consist of?

N. H. Taylor: This is a motor-driven potentiometer in the field of a generator which supplies the filaments.

W. J. Wachter: Is it only the filament you turn on slowly?

N. H. Taylor: The power supplies are turned on in a time sequence, but there is no attempt to turn them on slowly.

S. Ruhman (Moore School of Electrical Engineering): You mentioned that low screen dissipation in your gate circuit was one factor which gave you long life. Would you comment on that?

N. H. Taylor: I can just pretty much give you the facts without being sure that this is the only reason. I have heard of people using this *7AK7* gate tube with greater dissipation on the screen circuits, about 2 watts, with poor results. The duty factor on our number one circuit is probably less than 10 per cent, so that the screen dissipation in the circuit is very low, about 0.2 watt.

This is the only factor I know of which may lead to this 100,000-hour life expectancy in our gate circuit.

* This joint discussion covers both this and the preceding paper by R. R. Everett on the Whirlwind I Computer.

The EDSAC Computer

M. V. WILKES

THE invitation to speak to this conference about the EDSAC was particularly welcome to me because the foundations of my knowledge of electronic computers were laid during a visit to Philadelphia in the summer of 1946 when I attended part of a course at the Moore School of Electrical Engineering. I began to sketch out the design for the EDSAC in Philadelphia immediately after the course, and when I got back to Cambridge I was joined by Mr. Renwick and experimental work was started. Most of the important design decisions were taken in the first half of 1947 and the machine did its first calculation in the summer of 1949. I would like you, therefore, when listening to what I have to say about the design of the EDSAC, to cast your minds back to the conditions existing in 1947 and to the state of development of the subject at that time.

The EDSAC is a purely binary, serial, electronic computing machine with an ultrasonic store. It uses 5-hole teleprinter tape, read by a photoelectric tape reader, for input, and a similar tape, or direct printing on a teleprinter, for output. The EDSAC works with a single address order code. It has about 3,000 tubes in all, including diodes.

The EDSAC

The store of the EDSAC was designed to have a capacity of 1,024 storage locations, each capable of holding a number with 16 binary digits plus a sign digit, but until recently only about half this capacity has been available. It is possible for the programmer to combine any two storage locations (provided that the first has an even serial number) to form a long storage location capable of holding a number of 34 binary digits plus a sign digit (equivalent to about 10 decimals). This is done by making one of the digits in the order of 1 instead of a 0. An order contains 17 binary digits and will therefore go into a single (short) storage location.

If the designer of a computing machine using a single address code does not provide some system of this kind he finds himself in difficulties over the choice of a fundamental word-length. If he chooses it to suit orders (which only require about 16 or 17 binary digits), he forces the programmer to make frequent use of double length arithmetic in order to secure adequate computing accuracy, whereas, if he makes it considerably greater, then the words are longer than is necessary for orders, and inefficient use of the store results. Most designers, therefore, choose a word-length of some 35–40 binary digits, and build some means into the machine whereby two orders may be stored in the space of a single word. The system of short and long storage locations used in the EDSAC has the advantage that the short storage locations provided are available for short numbers as well as for orders. The arrangement has worked out very conveniently in practice and it is a feature I would be in favor of retaining in future machines.

The fundamental input operation in the EDSAC, that is, the operation called for by a single input order, is to read the next row of holes on the tape and to place the resulting 5-digit binary number in the store. This system differs from that used in some other machines, in which the basic input operation is to read ten or more rows of holes at a time. Our system has the advantage that the rows of holes on the tape are not divided up into arbitrary groups but can be used as the programmer thinks fit. It also makes the construction of a subroutine for converting numbers from decimal to binary form very simple. The decimal digits are punched as separate rows of holes and taken into the store one by one. The arithmetical operations necessary for converting the number to binary form are performed between the reading of the successive rows of holes, using the same group of orders each time. There is no need to punch nonsignificant zeros as there would often be if a fixed number of rows of holes on the tape corresponded to a single word inside the machine; for example, if the programmer has a sequence of 7-decimal numbers to put into the machine, it is not necessary, provided he uses an appropriate input subroutine, for him to punch zeros before the seven digits in order to make the number up to (say) 10. If he has a set of numbers of varying lengths to put in, he can use a subroutine designed to read numbers of any number of digits (up to 10), the end of the number being indicated by a special symbol, say a + or − sign, punched at the end.

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Input of Orders

I can further illustrate the flexible nature of the input system by describing the way in which orders are punched. First there is a letter indicating the function of the order, for example, A for add, S for subtract, et cetera. This is followed by the address in decimal form, nonsignificant zeros being omitted (for example, 51 not 0051). Finally there is a code letter which can indicate one of a number of things. The code letter "F" indicates that the address refers to a short storage location, while the code letter "D" indicates that it refers to a long storage location. Other code letters indicate that the address has to be modified by having a number held in a certain storage location added to it before the completed order is placed in its final location in the store. This facility is very useful in that it enables the programmer to make use of systems of relative numbering. The process of reading orders punched in the way just described is carried out by the machine under the control of a special subroutine known as the "initial input routine" which is permanently wired into the machine on a set of rotary switches and is placed automatically in the store when the starting button is pressed.

The input system of the EDSAC enables the programmer to write his orders in a form which is more adapted to his purpose than the binary form in which they exist in the store of the machine. It thus helps to avoid difficulties which would otherwise occur because of the conflicting requirements of the programmers and the engineers. Note that these advantages are obtained by building the machine with a specially simple input system, namely one which reads a single row of holes from the tape at a time. An input system in which groups of holes were read in one input operation would not only be more complicated mechanically, but it would be less convenient in practice.

The arithmetical orders provided in the EDSAC cover the operations of addition, subtraction, multiplication, and shifting of the number in the accumulator to the right or left. The accumulator holds 70 binary digits plus a sign digit and the result of a sequence of any number of additions, subtractions, and multiplications can be formed in the accumulator provided, of course, that an overflow does not occur. Products also can be subtracted from the number in the accumulator. A

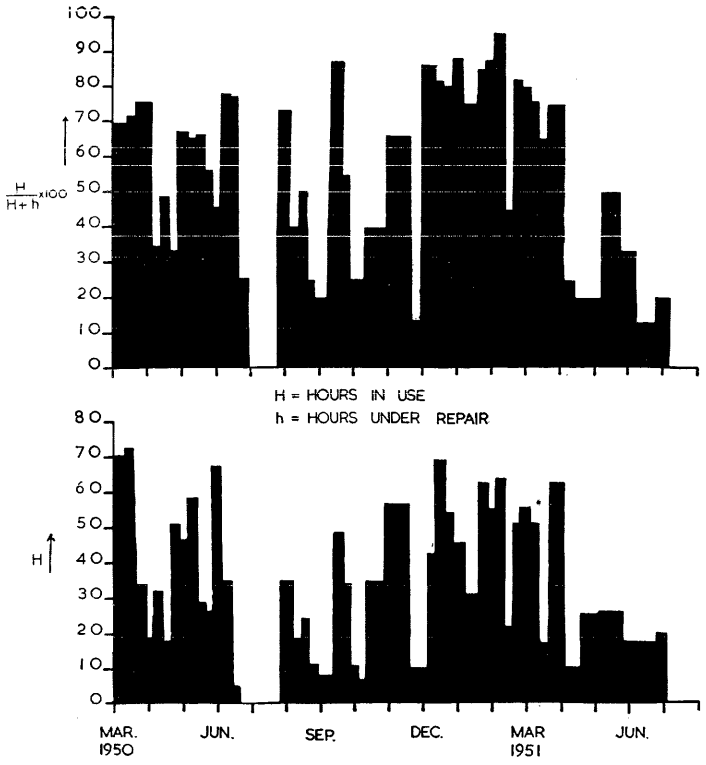
separate order is provided for placing a number in the multiplier register where it remains until it is replaced by another number. A separate round-off order is provided which adds a 1 into the 35th binary place of the accumulator. It is not convenient to combine the round-off order with multiplication in a machine which allows unrestricted accumulation of products in the accumulator, since round-off is only required if the number is to be transferred to the store immediately after the multiplication. It would have been possible to combine the round-off order with the order which transfers a number to the store, but since there are two such orders (one which clears the accumulator and one which does not) this would have involved the provision of two extra orders. The provision of a separate round-off order was more convenient from the engineering point of view and there is something to be said for it from the programming angle, since round-off is an important operation in numerical analysis and is quite worthy of the dignity of a special order. Whether, however, we would adopt the same system in another machine would depend on circumstances.

No divider is built into the EDSAC and division is performed by means of a subroutine. The decision not to build a divider was taken in order to simplify the structure of the machine. I cannot say that we have found the omission any great inconvenience but I think that we would probably include a divider in another machine.

Checking Devices

There are now no built-in checking devices in the EDSAC. It is left to the programmer to devise such checks as he thinks necessary. Until recently there was one checking device which enabled the programmer to check the operation of the printer. This was an order (known as the F-order) which caused the 5-digit number which had been passed to the teleprinter by the last output order to be read back into the store. This order was used in output subroutines in conjunction with a sequence of orders which verified that the number read back was correct. The provision of the F-order made the output system twice as complicated as it would otherwise have been, and twice as many faults in this part of the machine were, therefore, to be expected. In fact, we got rather more than this, since in order to make it possible to read numbers back from the teleprinter it was necessary to fit a set of five contacts in a somewhat confined space, and these were inclined to give trouble. The F-order has now been removed and a logical system of checking substituted. This was done by changing the teleprinter code to one in which the 10 decimal digits are all represented by 5-digit binary numbers containing two 1's and three 0's; previously they were represented by the binary numbers 0 through 9. A failure in the output system is now shown up by the printing of some symbol which is not a decimal digit, except in the unlikely event of two compensating failures occurring at the same time. This system of checking—which is, of course, well known and in use elsewhere—has the advantage that it will also show up errors introduced when tapes are copied.

Figure 1. Serviceability chart for the EDSAC



Another checking device included in the EDSAC in its early days was an alarm which sounded when the capacity of the accumulator was exceeded. This, however, turned out to be more trouble than it was worth, since there are a good many occasions, particularly when orders are being modified, when the programmer wishes to perform some operation which will necessarily involve an overflow in the accumulator. Another disadvantage was that the alarm tended to get switched off during testing operations, and not switched on again, so that it failed to serve the purpose for which it was intended. In consequence of these objections the device was removed from the machine.

You will perhaps wish me to say what attitude my experience with the EDSAC would make me take to checking devices in a new machine. I am, as you will have gathered from my remarks about the F-order, suspicious of devices which complicate the machine and therefore decrease its reliability. Perhaps this objection will diminish in force as technical progress makes machines more reliable, but of course such progress will also make checking devices less necessary. An electronic machine, when in correct working order, should not produce transient faults of the type familiar in relay machines and we do not find it necessary to incorporate what I might term detailed checks in the programme; for example, we do not programme each multiplication twice over with multiplier and multiplicand interchanged and check that the products agree. The checks we use are more of an over-all kind and depend on the nature of the problem being tackled. As far as the final results are concerned, such checks will always be necessary, if only to make sure that no error in mathematical formulation or in programming has been made, and no conscientious numerical analyst would be easy in his mind without them. On the other hand, in many problems there is a good deal of intermediate, or exploratory, work which it is perhaps not worth while to check at all, or for which a partial check can be accepted.

Testing the Machine

For testing the machine we have a collection of test problems which can be put

on at frequent intervals and whenever the operator suspects that the machine is not working correctly. The fact that the EDSAC can be changed over from one problem to another merely by putting another input tape into the tape reader, makes it convenient to do fault finding on test problems rather than on the actual problem being solved. Some of the test problems are designed to help the engineers find out what is the matter with the machine; others, if they are correctly performed, satisfy the operator that the machine is working correctly, but if they fail give no indication of what is wrong. I may say that we have found that it is not as easy as it sounds to make sure that the machine is in working order. So many different combinations of numbers can occur, and the machine can take up so many different operating rhythms according to the locations in the store of the various orders and numbers being used, that it is quite possible for a short problem designed to test each order to go through successfully and yet for a longer problem involving some minutes of computing time to fail. The most rigorous test program we have at the moment is one which was designed by Dr. David J. Wheeler for the purpose of testing whether a certain large number was prime or not. The number did turn out to be prime and for several days held the world record for the largest prime number known. It was then superseded by an even larger number tested by a similar program. That the program has survived as a test programme shows that even the theory of numbers has its uses.

The fact that in a reasonable space of time a machine can be tested only in a small proportion of its possible configurations constitutes a fundamental difficulty and in theory one is never justified in asserting categorically that a machine is in perfect working order. In spite of our experience with the EDSAC, however, I consider that it should be possible—and indeed others may have done it—to design and build machines in which the point is of little practical importance. Realization of the difficulty is, however, likely to influence one's views about the best form of logical design for a machine.

Having given a brief description of the logical structure of the EDSAC, I will now say something about the way in which that structure has been realized physically. During the whole of the time we were building the machine we had in mind the importance of pushing forward as rapidly as possible to the point at which we could begin to do experiments in programming and begin to run problems. This meant that we were not concerned with trying to arrive at the best engineering design for the various parts but rather at a satisfactory design. This point of view was, of course, engendered by the fact that we were a mathematical laboratory rather than an engineering laboratory.

Mercury Tanks

In order to ease the problems involved in designing the storage and computing circuits, a clock pulse repetition rate of 500 kc per second (giving a pulse interval of 2 microseconds) was chosen, although this was rather lower than what was being projected elsewhere. I do not think that we have ever regretted this decision as far as the EDSAC is concerned, but I think that we would feel sufficiently sure of our technique to use a somewhat higher pulse rate in a new machine. The tanks of the main store are about 5 feet long and give a delay of 1 millisecond. They are constructed from mild steel tubing and built in batteries of 16. Two such batteries have been built. In order to avoid difficulties in making the mercury wet the crystals, the tanks are filled with alcohol before the mercury is poured in. The alcohol is displaced but leaves a thin film on the surface of the crystals which provides acoustic contact with the mercury. Rubber washers are used for sealing. We have found that these batteries are very satisfactory in action, although there is a slow chemical action between the sulphur in the rubber and the mercury. It is therefore necessary to dismantle the batteries and clean them every two or three years. The crystals at the transmitting and receiving ends are matched into 80-ohm coaxial cables which connect them with the electronic circuits. Since they are matched the losses in these cables are small and they may be two or three yards long without causing difficulty. One advantage of separating the tanks from the electronic equipment is that since no heat is produced near the tanks themselves the temperature control problem is simplified. When the machine was first built no thermostat was provided, the battery—one only was in action—being placed inside a box which was partially lagged thermally. It was found that the temperature of the tanks remained sufficiently uniform, although it changed gradually with the ambient temperature of the room. The procedure was to adjust the clock pulse frequency from time to time to allow for this. The system was rather unsatisfactory, although less so than might have been expected, and the batteries were later placed in a temperature controlled oven. The clock pulses are derived from a highly-stable tunable oscillator of the Franklin type, kindly provided by Marconi's Wireless Telegraph Company Limited.

In addition to the long tanks used in the main store, the EDSAC contains nine short tanks with a delay of either half or one minor cycle. (A minor cycle corresponds to the duration of two short numbers.) One is used in the arithmetical unit to hold the multiplier, and another to hold the multiplicand. The accumulator consists of two short tanks connected in series, each capable of holding one long number. This is done so that access to the most significant half of a product can be obtained in each minor cycle. One short tank is used to count the required number of steps during multiplication or shifting operations. Another, connected in series with a half-adder through which a pulse is added in each minor cycle, is known as the counter tank and is used in conjunction with the access circuits of the store. Another short tank, also provided with a half-adder, is used to contain the address of the next order to be executed. From what I have said, you will see that in the EDSAC orders and numbers are handled in dynamic form wherever possible. In particular, the least significant digits of the address in the order being executed are passed in dynamic form to a "coincidence unit" where they are compared with pulses, also in dynamic form, coming from the counter tank, which I referred to just now. The coincidence unit produces a waveform which is used to operate gates leading to or from the store at the right times. Those digits of the order which need to control decoding trees cannot, however, be dealt with in dynamic form and they are used to set up flip-flops in a static register.

When first designed, the EDSAC contained several hundred relays, mostly connected with the input and output circuits.

Our experience is that, because of the inevitable bounce which occurs when mechanical contacts are closed, relays and electronic circuits do not work happily together and most of the relays in the EDSAC have now been removed. The replacement of the mechanical tape reader by a photoelectric tape reader enabled all the relays associated with input to be removed. The electromagnet which operates the ratchet for advancing the tape is connected directly in the anode circuit of a tube controlled by a flip-flop. A mechanical contact on the armature (this contact is heavy enough also to act as a mechani-

cal stop) is used to reset the flip flop. It does not matter if this contact bounces. On the whole the photoelectric tape reader has been a great success. It is simpler and more reliable than a mechanical one and, of course, considerably faster.

Auxiliary Equipment

A feature of the methods we have developed in the Mathematical Laboratory for running problems is the use of an extensive library of subroutines. The use of subroutines, both taken from the library and specially constructed, enables the program to be organized on several levels. In addition to subroutines of the more obvious sort, for example, those for evaluating standard functions such as sines and cosines, there are subroutines for performing quite sophisticated numerical operations, such as the numerical integration of a set of simultaneous nonlinear differential equations. It would be out of place in a lecture devoted to engineering topics to go into details about the library, but I might say something about the importance we attach to the provision of convenient and reliable equipment for preparing the programme tape. Apart from keyboard perforators, the main pieces of equipment provided are:

1. A duplicator, by means of which tapes may be copied, or a number of short tapes combined to form a single tape. This can be used for copying library tapes on to a programme tape. It also has facilities for incorporating corrections into a tape as it is being copied.

2. A comparator, or a device for verifying that two tapes are identical.

3. Equipment for printing output tapes taken from the EDSAC.

It is possible to have special equipment for verifying that tapes have been correctly punched, but we have found that in the particular circumstances of our Laboratory, a system of double punching and subsequent mechanical verification is quite satisfactory. At present all our tape preparation equipment uses mechanical tape readers (of our own design) and relays (mostly of the Siemens' high-speed type). We plan, however, to replace these with equipment using photoelectric tape readers and hard vacuum tube circuits. The object of this is not to get increased speed as much as improved reliability. Our experience with the photoelectric tape reader on the EDSAC has shown that it is very reliable and simple, and there is plenty of evidence to show that vacuum tube circuits designed for slow operation can be extremely reliable.

Serviceability

Tube Failures

The principal tubes used in the EDSAC are as follows:

EF54 (*CV1136*) (Mullard)	High slope pentode with maximum anode dissipation of 3 watts
EF55 (*CV173*) (Mullard)	High slope pentode with maximum anode dissipation of 10 watts
EA50 (*CV1192*) (Mullard)	Diode
EB34 (*CV1056*) (Mullard)	Double diode

These are normal sized tubes with the exception of the *EA50* which would now be called a miniature, although it was actually introduced when high definition television broadcasting started in 1936. Most of the *EF54*'s are triode connected and used as cathode followers, although a few are used as radio-frequency amplifiers in the storage circuits and as pulse amplifiers elsewhere. Most of the pulse amplifiers are of the cathode coupled variety. The reason for using pentodes connected as triodes was that a large supply of *EF54*'s was presented to the Laboratory by the Ministry of Supply immediately after the war. A good many of the *EF55*'s are also used as cathode followers in places where a larger power output is needed, but some of them also are used as pulse amplifiers. About one third of the diodes are used in diode gate circuits and the rest as d-c restorers or clampers.

The heaters are switched on in three stages, the whole operation taking about 2 minutes. This is done in order to reduce the thermal stresses during switching, but whether it does any good I cannot say. It is certainly true that heater failures are exceedingly rare, most of our tubes failing by becoming soft or by losing their emission completely. We would like to be able to try the effect of leaving the heaters on continuously whether the machine is in use or not, but we are not unfortunately in a position to provide the necessary supervision to guard against the fire risk. The heaters are, therefore, switched off whenever the machine is closed down.

Tube failures have tended to get fewer and fewer since the machine was first put into operation. Table I shows failures during two different periods. The tubes were by no means new at the beginning of the first period which was when we first began to keep systematic records. The figures in brackets underneath each tube type give the number of that particular type in use.

I would not like too great a significance to be attached to these figures, which have been extracted from the operational log book, since they refer to a collection of tubes of different ages and used under very different working conditions, some being lightly loaded and a few perhaps slightly overloaded. The decided fall in the failure rate from one period to the other confirmed an earlier impression that the failure rate was falling. *EF55*'s have a failure rate (if allowance is made for the relative numbers in the machine) about five times that of the *EF54*'s. I am inclined to believe that this is mainly because the *EF55* is inherently less reliable, although it is no doubt partly accounted for by the fact that *EF55*'s are only used in positions where a fairly large anode dissipation is necessary, whereas many of the *EF54*'s are loaded very lightly. During the first period the diodes showed an extremely small failure rate and this was a feature of our operational experience which stood out during that period. During the second period the failure rate of *EB34*'s increased slightly, but in view of the small numbers involved I would not like to say whether this is a real effect or an accidental one. It is rendered more conspicuous by the fact that the failure rate for the pentodes fell considerably. I think that one would expect diodes to be more reliable than pentodes because, in circuits used in a computing machine, the power dissipated at their anodes is so much less. Moreover, the electrode structure is simple and does not call for close spacings. Originally, the machine contained no germanium diodes, but a few have lately been incorporated.

Component Failures

Taken together, figures for the second period imply that in the EDSAC less than one tube failure occurs every two weeks. The number of failures of components other than tubes is comparable. During the period March 1950 to July 1951 about

Table I

Period	Hours Switched On	EF54 (1,150)	EF55 (200)	EA50 (750)	EB34 (600)
August 1949 to March 1950	1,400 (approx.)	11	12	1	1
April 1950 to July 1951	3,300	6	5	2	5

five mica condensers became short circuited, and about 20 resistors failed, either by becoming short circuited or open circuited, or by changing seriously in value. During that period we also found approximately 20 faulty soldered connections.

It is my impression that faults of the latter type have increased during the period the machine has been in operation, and it is possible that joints which appeared to be quite satisfactory when freshly made have become corroded with the passage of time. In a new machine we would arrange for all the soldered joints to be accessible when the units were removed from the machine. Moreover, the wires would not be twisted around the soldering tags before soldering but would be merely laid against them. The mechanical strength of a joint would then reside entirely in the solder and the joint would tend to fail completely rather than become noisy. At any rate it would be quite easy to test whether a joint was sound by pulling the wire with a pair of instrument forceps.

It would be satisfactory if all the faults on the EDSAC were due to the failure of a tube or a component, but this is by no means the case. Many faults in the past have occurred as a result of a marginal condition occurring in some part of the machine and have been cured by an amplifier adjustment. Such a state of affairs suggests that the circuit design is not everywhere ideal. The policy has always been to make modifications to the circuits, or to rebuild individual units, if it were thought that a greater degree of operating tolerance could thereby be achieved, but, until recently, nothing very extensive along these lines was attempted, since it was desired to avoid putting the machine out of action for a long period. It is always difficult to know whether to work on the machine to make it more reliable, or to try to keep it in working order with as little interruption as possible so that the users can get on with their work. Our policy was rather to favor the users, and I think that while they were, for the first time, getting experience of high speed computing methods and establishing a library of subroutines, this was the right policy. However, in July 1951, we decided that the time had come to take the machine out of service for a general overhaul and partial rebuild. Our circuit technique had improved in a good many ways since most of the circuits were designed, and there were many places in which we could improve on our earlier designs. The machine has been put into service again during the last few weeks and we have every reason to believe that serviceability will be a good deal better but I am afraid it is too early to give you any figures.

The conditions under which we operate make it rather difficult to give figures for the serviceability of the EDSAC which are not in some way or other misleading. The machine is operated during ordinary laboratory working hours with the maintenance staff in attendance. If it is serviceable it is also available for use in the evenings and during the night by members of the mathematical staff and by graduate students. No maintenance engineers are, however, present so that if the machine breaks down, even for a trivial reason, it has to be abandoned. This must be remembered when interpreting figures for the percentage of time the machine was serviceable. The number of hours per week during which it was serviceable is perhaps a better guide, but a low figure in any week could indicate either that the machine was working badly, or that there was a shortage of people who were willing to work through the night.

Discussion

E. C Berkeley (Edwin Berkeley and Associates): I would like to ask Professor Wilkes about what was the cost of his machine, including some kind of value for the various gifts from the Government and others.

M. V. Wilkes: I wish I could answer that question. To be quite honest, we never worked it out, since it was the outcome of a development program. In a university, unless you go to a certain amount of trouble, overheads tend to get submerged, and it would not be easy to give a figure which would mean anything. The machine has about 3,000 tubes in it. You can work out roughly for yourself what that amounts to in bits and pieces.

E. C. Berkeley: Could you perhaps locate it as near $100,000, or near $500,000, or near $1,000,000?

M. V. Wilkes: I would rather not be drawn out on this, but it is less than $1,000,000.

H. W. Berry (Minneapolis-Honeywell Regulator Company): I am interested in the photoelectric tape reader which you described very briefly. Could you elaborate a bit more on it? Is it a commercial device or one you developed?

M. V. Wilkes: It is a device we developed ourselves. It uses a ratchet mechanism, the same kind of ratchet mechanism as used in telephone switches. The optical system is an extended one. You saw it was in rather a tall box. A light shines through the holes in the tape and forms an enlarged image of them on five photocells placed at the bottom of the box. Small photocells that could be put behind the hole were not available when it was designed.

The ratchet is worked directly from the anode of the tube, controlled by a flip-flop. There is a contact on the armature, which resets the flip-flop directly, so that no relays are involved.

We found that the elimination of relays and the general simplification of the circuits which arise from using a photocell tape reader increase the reliability of that part of the machine a great deal. And I think it has been in every way a great success. It will step as quickly as 50 rows of holes a second. You did not see it going at that speed because in our system we usually do a certain amount of calculation between the readings of rows of holes; for example, a decimal number such as an address is converted to the binary ststem by operations performed between the readings of the rows of holes.

T. K. Sharpless (Technitrol Engineering Company): I want to ask about the monitor tubes we saw in the movie. Do they prove to be a very useful device for checking your memory and its operations?

M. V. Wilkes: Yes, the monitor tubes are certainly very useful. Of course, one advantage of a serial machine is that you can quite easily get a monitor to show you the whole contents of a section of the memory. You don't have to get one digit from one tube and another from another tube, and so on.

J. H. Wright (National Bureau of Standards): You said that you did not have a marginal checking scheme. Do you have a routine checking scheme?

M. V. Wilkes: I would say we do not. On the whole we try to do a certain amount of preventive maintenance from time to time. But we do not have any organized system, and certainly I think in a new machine we would have marginal checking and a regular routine of preventive maintenance.

The National Bureau of Standards Eastern Automatic Computer

S. N. ALEXANDER

SOME of you undoubtedly recall hearing reports during 1949 on the progress of the Interim Computer at the Washington Laboratory of the National Bureau of Standards. The program to develop that computer was proposed and explored during the summer of 1948 as means for providing a "stop-gap" installation for the NBS Computation Laboratory during the interim period while full scale equipment from a commercial source was being completed for delivery. This point of view was retained up to the end of 1949, during which period the machine's system and circuitry were developed. Early in 1950, however, it became evident that this "stop-gap" equipment would be the only equipment that would be available for two, and possibly three years. In view of this, the ultimate objectives for the computer installation were raised to cope with what could no longer be considered "an interim situation." Furthermore, the name "Interim Computer" was no longer appropriate and was eventually replaced by "SEAC"—Standards' Eastern Automatic Computer.

Summary of Program

Although the ultimate objectives for the complete SEAC installation were raised, we still wanted to try for an initial installation that was not much above that for the interim computer. The prime objective was still to get into operation, at the earliest possible date, a modest performance high-speed digital computer to satisfy the initial requirements of the NBS Computation Laboratory. However, the requirement of the development program of the Electronic Computers Laboratory introduced a second aspect to the SEAC program. We needed an effective experimental tool for evaluating advances in computer components and systems. In order to reconcile these somewhat conflicting requirements, it was planned that the SEAC should be made expandable, that is, should consist of a central nucleus, with high priority on early completion, to which additional equipment could be added at a later time. These additions would be included as time permitted or as operating experience dictated.

The central nucleus of the SEAC was put into regular operation in May 1950, approximately 20 months after the engineering work began. A complete chronology of the SEAC program is given in Table I. At the time of its dedication, SEAC was a completely serial machine operating at a basic repetition rate of 1 megacycle per second, and it contained:

1. A memory unit of 512 words stored in 64 acoustic mercury delay lines (average access time: 168 microseconds).
2. An input-output unit consisting of teletype punched paper tapes and modified teletype keyboard and page printer.
3. A control unit operating with a 4-address instruction word consisting of 45 binary digits.
4. An arithmetic unit capable of performing addition, subtraction, multiplication, division, a type of extract operation called "logical transfer," and two types of comparison operation (sometimes called discrimination or branch operations).

Summary specifications for the original SEAC are listed in Table II.

The interval following the dedication of SEAC was devoted to tidying up construction changes introduced during the 3-month period of testing and adjustment, and to solving problems as rapidly as they were prepared. By October 1950, things had settled down and we initiated a regular schedule of operation in which machine time was distributed among problem-solution, engineering modifications (to expand the installation) and preventive maintenance. We began keeping detailed records of SEAC's operation, both to obtain engineering information and to determine whether the initial charge of $80 per hour of good computation was adequate to cover the costs of maintenance service and the repair and upkeep of the equipment.

In October 1950, the program for the expansion of SEAC began in earnest, with the annexation of equipment for an additional 512 words of electrostatic memory using the Williams' mode of storage. This expansion work has continued up to the present time and the electronic equipment is essentially all installed. However, we still plan to connect and use a wide variety of input-output devices with SEAC, as part of our development program. In its present condition, the installation now contains the following new equipment:

1. An additional 512 words of electrostatic memory, now in trial operation, with over 300 hours of productive computation completed.
2. Additional input-output units consisting of two high-speed magnetic tape drives operating under the internal control of the machine; two magnetic wire drives for high-speed loading and unloading of the machine, operating in conjunction with an inscriber and outscriber for transcribing to and from punched paper tape and magnetic wire; and an external selector used in conjunction with all of the input-output equipment for controlling up to ten different units.
3. Additional control units consisting of an Automonitor for automatically printing out, at the option of the operator, selected instructions and the results of their execution; and a 3-address control unit containing special features for automatizing certain programming operations. (This equipment is installed and tested but not yet in regular use with the entire machine.)

Summary specifications for the expanded SEAC are listed in Table III.

The physical appearance of the computer is illustrated in Figures 1 through 4. Figure 1 gives a general view of the machine from the operator's side and includes a view of one of the high-speed magnetic tape-handling devices. The other side of the machine has a similar appearance and contains the electrostatic memory, a part of which is shown in Figure 2. The acoustic memory is in a separate cabinet, which is shown in Figure 3.

Table I. Chronology of SEAC

March to October 1948	Study of operational requirements and general machine organization
October 1948 to December 1949	Development of machine system, circuitry, and construction techniques
September 1949 to March 1950	Construction of SEAC "nucleus"
March to May 1950	Adjustment and test period
May 9, 1950	Solution of first significant problem: skew ray problem for the NBS Optics Division
June 20, 1950	Announcement and dedication of machine
June 1950 to Present	Utilization of machine for solution of problems, and expansion of machine by annexation of additional equipment to the original "nucleus"

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The author wishes to express his appreciation to the staff of the NBS Computation Laboratory for the assistance received in compiling this data.

Table II. Specifications for SEAC "Nucleus"

Operation	Average Time in Microseconds for Complete Operation* (including Access Time)
Addition	864
Subtraction	864
Multiplication	2,976
(a) Major part, unrounded	
(b) Major part, rounded	
(c) Minor part	
Division	2,976
Logical Transfer	864
(An arbitrary partial word transfer for the purpose of forming composite words)	
Comparison	696
(A conditional transfer of control based on value of arithmetical result)	
(a) Algebraic value	
(b) Absolute value	

Components	Total Number in SEAC Nucleus
Vacuum tubes	747
Germanium diodes	10,500
Electrical delay lines	394
Acoustic delay lines	64

* A complete arithmetic operation consists of reading the instruction word and two operands out of the memory, and writing the result back into the memory. Access time thus includes four arbitrary references to the memory. These figures are for operation with the acoustic memory.

Table III. Expanded SEAC Specifications

Operation	Average Time in Microseconds for Complete Operation* (including Access Time)
Addition	240
Subtraction	240
Multiplication	2,350
(a) Major part, rounded	
(b) Major part, unrounded	
(c) Minor part	
Division	2,350
Logical Transfer	240
Logical Multiplication	240
Comparison	192
(a) Algebraic value	
(b) Absolute value	
Base	192
(An order for automatically modifying addresses and/or for conditional transfer of control)	
File	192
(An order for writing contents of control counter register into the memory)	

Components	Total Number in Expanded SEAC
Vacuum tubes	1,290
Germanium diodes	15,800
Electrical delay lines	654
Acoustic delay lines	64
Electrostatic storage tubes	48

* These figures are for operation with the electrostatic memory only.

An interior view is visible in Figure 4, showing the plug-in components—diode clusters, pulse transformers, and enclosed electrical delay lines. The push-on interconnecting wires for carrying the high-speed pulses from chassis to chassis also are visible.

Table IV. SEAC's Operating Record for an Average Week

	Number of Hours	Percentage of Total Time	
Assignment			
Scheduled for preventive maintenance	20	12%	based on 168 hours per week
Scheduled for problem-solution	83	49%	
Scheduled for engineering	52	31%	
Total for all purposes	155	92%	
Unscheduled	13	8%	
Operating Performance			
Productive time			
for problem-solution	54	65%	based on 83 hours per week
for engineering	43	83%	based on 52 hours per week
Unproductive time			
(Machine out of order)	31	20%	based on 155 hours per week
Idle time			
(Machine in order)	7	5%	
Total	155	100%	

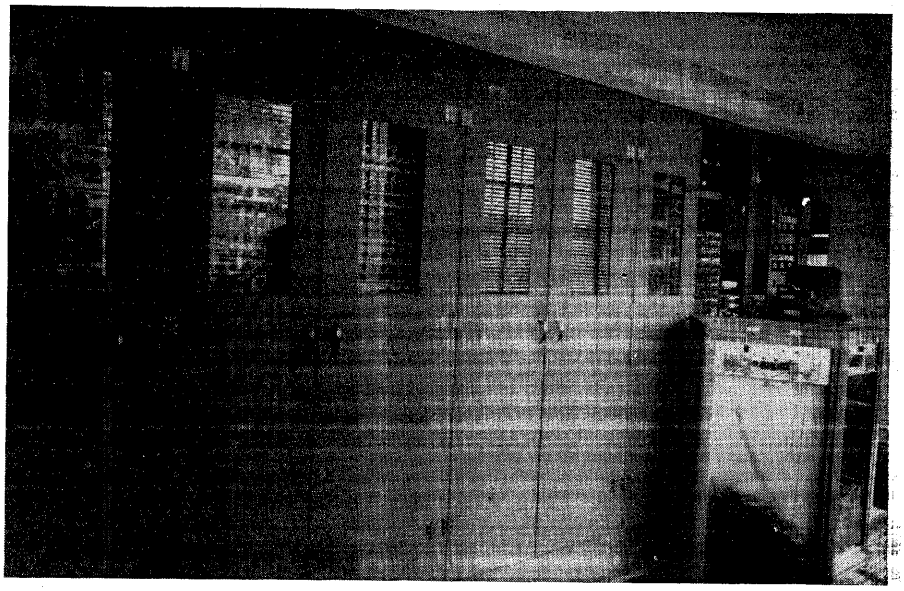


Figure 1. General view of SEAC

At this point it might be advisable to mention some of the particular deviations from normal techniques that are present in SEAC. The most important are:

1. Germanium diodes are used for practically all switching functions. Details of this technique are given in Figure 5.

2. One type of vacuum tube is used in almost all of the high-level pulse circuits. It is a miniature beam tetrode, the *6AN5*.

3. Step-down pulse transformers are used with each vacuum tube to provide a-c coupling between switching circuits, for impedance matching, and to provide output signals of both polarities.

4. A combination consisting of a single tube, pulse transformer, and 1 microsecond of electrical delay is used to replace the usual Eccles-Jordan type of flip-flop for single digit storage. This provides a-c outputs of both polarities, having ample drive to provide the control functions on other parts of the computer. It also is the basic element for our shift register and binary counters.

5. The availability of low impedance drive out of the transformers, together with suitable use of diode clamping and disconnecting techniques has reduced cross-talk effects between circuits. Thus, it has been unnecessary to shield or space the open wires between chasses, despite the 15-volt signals at a 1-megacycle repetition rate and the 0.1-microsecond rise and fall of these pulses.

Summary of SEAC Operating Record

In order to handle the work load involved in solving problems, expanding SEAC, and evaluating newly installed equipment, it became necessary to utilize the computer 24 hours per day, seven days a week. Of the 168 hours available, it was planned to allot 76 hours to problem-solving, 76 hours to engineering, and 16 hours to preventive maintenance.

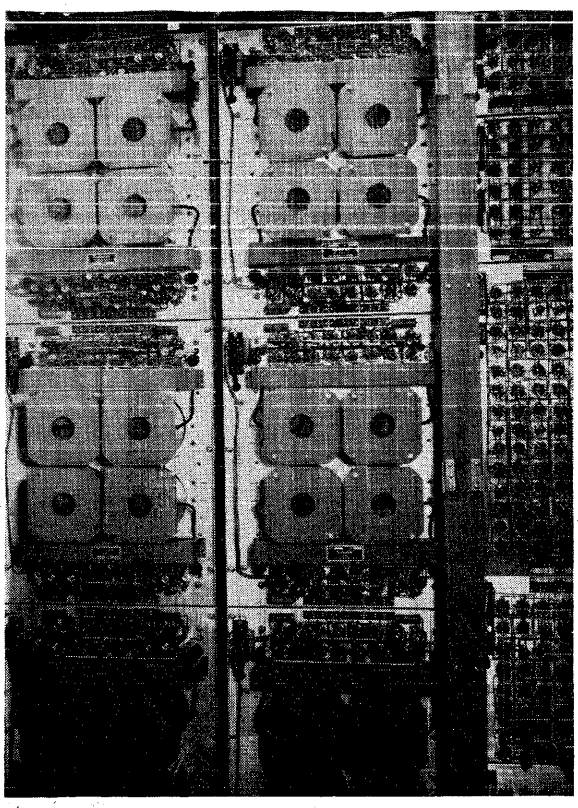


Figure 2 (left). Part of the electrostatic memory

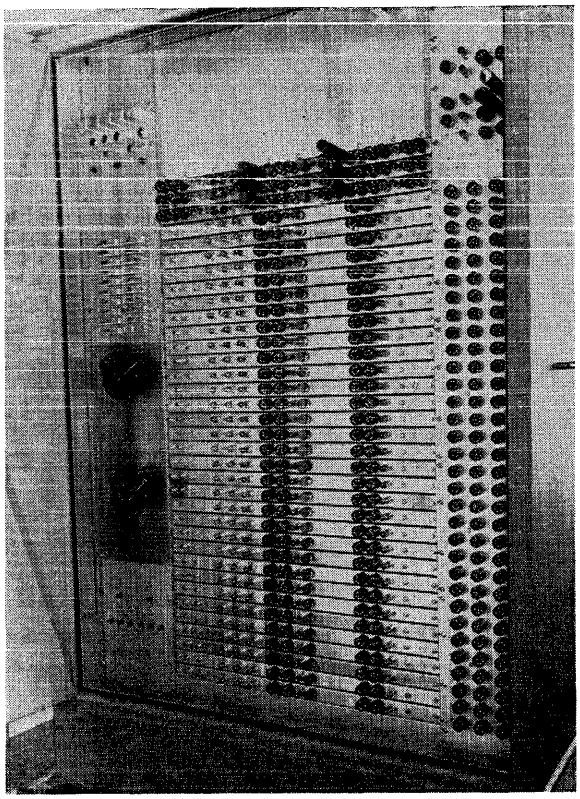


Figure 3 (right). Acoustic memory cabinet

We now have the complete records for a full 12 months of scheduled operations. A week-by-week breakdown is given in Appendix II. Table IV summarizes the SEAC's operating record for an average week, and provides an indication of the machine's serviceability as well as of the intensity with which it was utilized during its first year, on over 60 different problems.

A list of these problems is given in Appendix I.

It should be borne in mind that the 54 hours of productive operation (out of the 83 hours scheduled for problem-solution) were logged in the midst of a steady expansion of our computing facilities. As these new facilities were put to work, there were usually brief bursts of lost time from both residual defects in the equipment and improper use of the new facilities.

It is a source of considerable gratification to remark on the fine teamwork between the designers and the users of SEAC, which contributed to the records given above. All this augers well for the day when we can settle down to normal operation, instead of the present schedule which necessitates pulling SEAC apart on two days of each week and then "zipping" it back together again in time for preventive maintenance and scheduled computation operation.

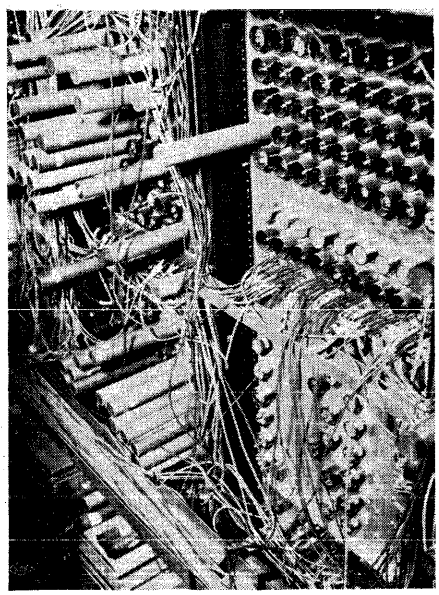


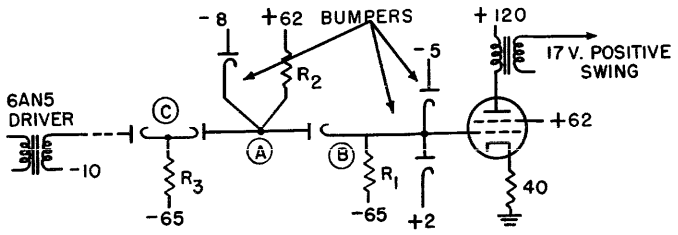
Figure 4 (left). Interior view of SEAC

Appendix I. List of Problems Worked on the SEAC

Mathematics and Statistics Problems

Computation of Function Tables

1. Table of the exponential function for negative arguments.
2. Table of the exponential-integral function for complex arguments.
3. Tables of hyperbolic sines and cosines.
4. Table of the error function for complex arguments.
5. Tables of Jacobi ellipic functions for real arguments.
6. Tables of coulomb wave functions.
7. Tables for Loran navigation.
8. Tables of power points for analysis-of-variance tests.



$R_3 < R_2 < R_1$

SIGNALS ARE ½ μ SEC PULSES, UP TO 1 MC. PRF.
ADDITIONAL AND INPUTS MAY BE TIED AT (A)
ADDITIONAL OR INPUTS MAY BE TIED AT (B) OR (C)
FEEDBACK, RECLOCKING, AND NEGATIVE PULSE CIRCUITS NOT SHOWN. USE SAME SWITCHING TECHNIQUE.

Figure 5 (right). Diode switching in SEAC computer

Table V. Problem-Solution Time

Week of	Total Hours Assigned to Problem Solution	"Good" Hours: On Problem Solutions	"Good" Hours: On Coding Checks	"Good" Hours: In Order but Idle	"Down" Hours: Debugging	"Down" Hours: Machine Error	"Down" Hours: Out of Order Idle	Good Portion of Total Problem Time Per Cent
October through December 1950								
Oct. 1	76	30	11	0	68*	30*	22*	54
Oct. 8	76	11	4	4	54*	28*	32*	25
Oct. 15	79	30	28	2	10	8	1	78
Oct. 22	74	56	9	1	0	8	0	89
Oct. 29	98	59	12	2	5	19	1	76
Nov. 5	76	35	5	0	21	15	0	53
Nov. 12	76	44	13	0	6	13	0	62
Nov. 19	64	25	25	4	3	7	0	84
Nov. 26	82	34	18	7	3	20	0	72
Dec. 3	77	55	10	2	6	4	0	87
Dec. 10	86	52	6	6	7	12	3	74
Dec. 17	58	44	3	3	0	8	0	86
Dec. 24	76	41	29	3	0	3	0	96
Totals	998	516	173	34	183	175	59	73
January through March 1951								
Dec. 31 (1950)	70	20	22	18	7	1	2	86
Jan. 7	109	50	35	1	12	11	0	79
Jan. 14	66	25	9	4	2	23	3	58
Jan. 21	96	26	22	4	16	24	4	54
Jan. 28	83	30	14	2	11	25	1	55
Feb. 4	89	9	34	0	19	22	5	48
Feb. 11	76	21	17	1	4	30	3	51
Feb. 18	76	35	15	2	4	10	0	82
Feb. 25	86	34	16	3	11	17	5	62
Mar. 4	83	30	10	2	15	25	1	51
Mar. 11	83	8	21	4	22	28	0	40
Mar. 18	111	38	29	3	2	30	9	63
Mar. 25	88	44	17	3	1	19	4	73
Totals	1,116	380	261	47	126	265	37	62
April through June 1951								
Apr. 1	59	17	3	2	7	19	11	37
Apr. 8	96	67	11	8	2	4	4	90
Apr. 15	95	63	17	6	4	5	0	91
Apr. 22	94	46	18	8	2	17	3	77
Apr. 29	87	27	10	9	6	16	19	53
May 6	88	16	26	12	7	19	8	61
May 13	112	73	17	6	2	14	0	86
May 20	97	39	26	10	1	16	5	77
May 27	110	56	23	4	3	11	13	75
June 3	96	33	29	7	0	18	9	72
June 10	44	6	10	0	3	13	12	36**
June 17	99	36	18	2	13	15	15	57
June 24	55	26	10	4	3	10	2	73
Totals	1,132	505	218	78	53	177	101	71
July through September 1951								
July 1	75	51	17	4	1	2	0	96
July 8	68	31	20	8	4	4	1	87
July 15	54	16	20	8	1	9	0	81
July 22	77	45	17	6	1	8	0	90
July 29	103	60	12	3	7	11	10	73
Aug. 5	82	42	6	8	0	14	12	64
Aug. 12	55	24	8	0	0	12	11	58
Aug. 19	79	21	40	1	4	10	3	79
Aug. 26	94	6	38	1	11	37	1	48
Sept. 2	95	24	49	4	6	9	3	81
Sept. 9	105	31	41	3	2	17	11	72
Sept. 16	90	58	15	3	0	10	4	85
Sept. 23	90	43	18	2	0	19	8	70
Totals	1,067	452	301	51	37	162	64	75
Grand Totals	4,313	1,853	953	210	399	779	261	70

* These figures include engineering time as well as problem-solution time.

** Installation of new, more flexible manual control.

Table VI. Engineering Time

Week of	Total Hours Assigned to Engineering Work	"Good" Hours: Engineering Time	"Good" Hours: In Order but Idle	"Down" Hours: Debugging	"Down" Hours: Machine Error	"Down" Hours: Out of Order Idle	Good Portion of Total Engineering Time Per Cent
October through December 1950							
Oct. 1		0	0				
Oct. 8		20	0				
Oct. 15	69	20	1	30	0	18	30
Oct. 22	74	43	9	9	4	9	70
Oct. 29	55	38	3	8	0	6	75
Nov. 5	70	50	1	19	0	0	74
Nov. 12	67	24	15	23	5	0	58
Nov. 19	62	55	2	0	4	1	92
Nov. 26	57	57	0	0	0	0	100
Dec. 3	57	56	1	0	0	0	100
Dec. 10	43	42	1	0	0	0	100
Dec. 17	54	40	7	7	0	0	87
Dec. 24	20	12	2	6	0	0	70
Totals	646	457	42	102	13	34	78
January through March 1951							
Dec. 31 (1950)	20	17	3	0	0	0	100
Jan. 7	11	10	0	1	0	0	91
Jan. 14	56	39	9	8	0	0	86
Jan. 21	51	49	1	1	0	0	98
Jan. 28	53	41	12	0	0	0	100
Feb. 4	59	58	1	0	0	0	100
Feb. 11	67	61	2	4	0	0	94
Feb. 18	84	84	0	0	0	0	100
Feb. 25	72	71	1	0	0	0	100
Mar. 4	66	66	0	0	0	0	100
Mar. 11	69	69	0	0	0	0	100
Mar. 18	28	28	0	0	0	0	100
Mar. 25	46	40	6	0	0	0	100
Totals	682	633	35	14	0	0	98
April through June 1951							
Apr. 1	45	33	12	0	0	0	100
Apr. 8	60	55	5	0	0	0	100
Apr. 15	54	51	0	1	2	0	94
Apr. 22	62	52	10	0	0	0	100
Apr. 29	61	61	0	0	0	0	100
May 6	68	68	0	0	0	0	100
May 13	46	43	1	2	0	0	96
May 20	63	48	14	0	1	0	98
May 27	34	34	0	0	0	0	100
June 3	37	37	0	0	0	0	100
June 10	114	77	32	5	0	0	95
June 17	55	29	0	26	0	0	53
June 24	61	29	7	25	0	0	59
Totals	760	617	81	59	3	0	92
July through September 1951							
July 1	28	28	0	0	0	0	100
July 8	59	38	0	21	0	0	65
July 15	69	69	0	0	0	0	100
July 22	57	57	0	0	0	0	100
July 29	33	13	0	20	0	0	39
Aug. 5	30	27	0	3	0	0	100
Aug. 12	56	36	0	20	0	0	64
Aug. 29	50	50	0	0	0	0	100
Aug. 26	47	47	0	0	0	0	100
Sept. 2	42	42	0	0	0	0	100
Sept. 9	32	32	0	0	0	0	100
Sept. 16	67	67	0	0	0	0	100
Sept. 23	68	68	0	0	0	0	100
Totals	638	574	0	64	0	0	90
Grand Totals	2,728	2,281	158	239	16	34	89

PROBLEMS IN NUMERICAL ANALYSIS

1. Solution of integral equations (Dirichlet problem) by iterative methods.

2. Solution of partial differential equations (Laplace equation) by Monte Carlo method.

3. Solution of partial differential equations (heat flow) by various methods in order to evaluate the effect of round-off error.

4. Inversion of matrices by various methods (including Monte Carlo).

5. Solution of Warschawski problem (conformal mapping) by numerical methods.

NUMBER THEORETICAL PROBLEMS

1. Tables of prime numbers, and primitive roots of primes.

2. Solutions of diophantine equations, et cetera.

PROBLEMS IN STATISTICS

1. Generation of optimum sampling plans for the Bureau of the Census, that is, determination of sampling procedures corresponding to minimum cost, minimum variance, et cetera.

2. Generation of random samples from a normal probability distribution and application of acceptance criteria to them.

Physics Problems

CRYSTAL STRUCTURE

1. Calculation of electron density in a cell

of a crystal from observed "structure factors."

2. Calculation of interplanar spacings in crystals for various lattice parameters in order to index X-ray powder diffraction patterns.

X-RAY AND GAMMA RAY PENETRATION

1. Solution of Volterra integral equations relating to radiation penetration in materials.

RELATIVE ABUNDANCE OF THE ELEMENTS

1. Solution of differential equations relating to the neutron-capture theory of the formation of elements in the universe.

INTERNAL CONVERSION COEFFICIENTS

1. Calculation, for the L-shell, of the ratio of the number of electrons to photons involved in the transition of a radioactive nucleus.

WAVE FUNCTIONS FOR HELIUM ATOM AND FOR LITHIUM ATOM

NEUTRON DIFFUSION PROBLEM

GEOMAGNETIC FIELD PROBLEM

1. Calculation of internal magnetic field of the earth from observations made at the earth's surface.

CELESTIAL MECHANICS PROBLEM

1. Calculation of orbits in the restricted three-body problem, that is, the motion of an infinitesimally small body in the gravitational field of two bodies of finite size.

HEAT-FLOW PROBLEMS

1. Calculation of the distribution of temperature inside a thermally reactive material.

2. Calculation of the conduction of heat inward from a surface exposed to high intensity radiation.

Engineering Problems

OPTICAL SYSTEM DESIGN

1. Calculations of the paths of skew rays through systems of lenses.

ELECTRONIC CIRCUIT DESIGN

1. Calculation of the starting transient in a class-C oscillator.

2. Calculation of the response of a nonlinear system to noise.

SYNCHROTRON DESIGN

1. Calculation of the effects of forced oscillations in the Brookhaven proton synchrotron.

ELECTROMAGNETIC ENGINEERING

1. Calculation of trajectories of electrons through a resonating cavity.

2. Calculation of magnetic fields generated in the neighborhood of electromagnetic devices.

FLUID DYNAMICS

1. Calculation of flow in supersonic nozzles.

2. Calculation of pressure distribution on bodies of revolution.

3. Calculation of the rolling moment due to side slip of an airplane wing.

Table VII. Other Time, and Summaries of Performance

Week of	Total Hours Assigned to Preventive Maintenance	Hours Idle in Order (Unassigned)	Total Hours "Good"*	Total Hours Assigned*	Good Portion of Total Time, Per Cent*
October through December 1950					
Oct. 1	8		41	76	54
Oct. 8	15		39	96	41
Oct. 15	20	0	81	148	55
Oct. 22	20	0	118	148	80
Oct. 29	15	0	114	153	75
Nov. 5	22	0	91	146	62
Nov. 12	25	0	96	143	67
Nov. 19	26	16	111	126	88
Nov. 26	21	8	116	139	84
Dec. 3	30	4	124	134	93
Dec. 10	14	25	107	129	83
Dec. 17	36	20	97	112	86
Dec. 24	26	46	87	96	91
Totals	278	119	1,222	1,646	74
January through March 1951					
Dec. 31 (1950)	32	46	80	90	89
Jan. 7	3	45	96	120	80
Jan. 14	37	9	86	122	71
Jan. 21	21	0	102	147	69
Jan. 28	24	8	99	136	73
Feb. 4	20	0	102	148	69
Feb. 11	25	0	102	143	71
Feb. 18	8	0	146	160	91
Feb. 25	10	0	125	158	79
Mar. 4	19	0	108	149	73
Mar. 11	16	0	102	152	67
Mar. 18	29	0	98	139	71
Mar. 25	34	0	110	134	82
Totals	278	108	1,356	1,798	76
April through June 1951					
Apr. 1	64	0	67	104	64
Apr. 8	12	0	146	156	94
Apr. 15	19	0	137	149	92
Apr. 22	9	3	134	156	86
Apr. 29	12	8	107	148	72
May 6	12	0	122	156	78
May 13	10	0	140	158	89
May 20	8	0	137	160	85
May 27	9	15	117	144	81
June 3	11	24	106	133	80
June 10	10	0	125	158	79
June 17	14	0	85	154	55
June 24	30	22	76	116	65
Totals	220	72	1,499	1,892	79
July through September 1951					
July 1	49	16	100	103	97
July 8	32	9	97	127	77
July 15	11	34	113	123	92
July 22	10	24	125	134	93
July 29	19	13	88	136	65
Aug. 5	18	38	83	112	74
Aug. 12	13	44	68	111	61
Aug. 19	18	21	112	129	87
Aug. 26	18	9	92	141	66
Sept. 2	7	24	119	137	87
Sept. 9	31	0	107	137	79
Sept. 16	11	0	143	157	91
Sept. 23	10	0	131	158	83
Totals	247	232	1,378	1,705	81
Grand Totals	1,023	531	5,455	7,041	77

* For both problem and engineering work.

4. Calculation of the pressure distribution and displacement resulting from a blast in an ideal gas under conditions of spherical symmetry.

MECHANICS

1. Calculation of the deflection of a column subject to plastic deformation.

2. Computation of sound-transmission integrals for single and double walls.

3. Tabulation of functions for facilitating determination of the shape and tension in a flexible cable held in a uniform stream.

Business Management and Economic Problems

PROBLEMS RELATED TO AIR FORCE PROGRAM-PLANNING

1. Computation of production-scheduling and procurement requirements for the Office of the Air Comptroller, United States Air Force.

2. Research in linear-programming theory, for example, solution of various systems of linear inequalities relating to "game" problems, "input-output" problems, transportation problems, et cetera.

PROBLEMS RELATED TO SOCIAL SECURITY ACCOUNTING PROCEDURES

1. Study and demonstration of sorting and tabulating processes.

Military Problems

In this category, approximately 20 classified problems were worked on the SEAC.

Appendix II. Statistics on SEAC's Operating Performance—October 1950 through September 1951

Table V contains details, for each week, of the computer's performance during the time set aside for problem-solution. Of this time, the "good" portion was that in which either (1) problem-solutions or coding checks were turned out correctly by the machine, or (2) the machine was in good operating order but it was idle.

"Down" time was that portion in which either (1) time was lost because of machine malfunctions during problem-solution (including the time used for rerunning problems, to permit continuation), or (2) machine malfunctions were being diagnosed and equipment debugged, or (3) the machine was out of order and idle. For the entire year, the "good" time was 70 per cent of the total time which was assigned to problem-solution.

Table VI gives the details, for each week, of machine performance during the time when the SEAC was assigned to engineering test and development work. Of this time, the "good" portion was that in which there was no malfunction of any machine which had previously been put into regular operation. For the entire year, the "good" time was 89 per cent of the total time assigned to engineering work.

Table VII accounts for the remainder of time and summarize the total good performance (both on problem-solution and engineering projects) for each week. The "good" time for the entire year was 77 per cent of the total time assigned to both projects.

(Discussion of this paper was combined with that of the following paper)

Engineering Experience with the SEAC

RALPH J. SLUTZ

FROM the time of its early planning phases the SEAC program at the National Bureau of Standards has had a dual purpose. One objective has been, of course, the provision of a tool for use in the solution of problems in calculation, but a second and equally important aspect is the use of this equipment to provide experience with which better tools can be designed in the future. Thus about one-third of SEAC's time during the past year has been used for the testing out of new equipment in order to obtain design experience for further development.

First let me mention that the decision to use a full-fledged computer as a piece of test equipment has been amply justified. The two major such uses have been in conjunction with the design and evaluation of a full electrostatic-storage memory and also with the design of several varieties of magnetic tape devices for use as input-output devices and as auxiliary memory. When working with such devices, we test them first in the laboratory as carefully as is feasible without constructing overly complex laboratory equipment. Then they are tried with the SEAC, and invariably their use as part of a full computing system shows up weaknesses which have been overlooked in the laboratory. When these weaknesses have been corrected, the unit is then used in regular problem computation, and it has been our experience time and again that the variety of use such a unit gets in handling a large number of problems turns out to be a much more rigorous test than any acceptance test we have been able to devise. Thus the computing system has proved to be a most valuable piece of test equipment, especially so because of the great flexibility of test programs possible simply by putting different routines in the machine. It appears clear that in order to achieve as good results with specialized test equipment as we do with the computer, this specialized test equipment would have to be nearly as complex as a full computer; and to be as flexible as the computer is, it would have to have a great many of the characteristics of a computer—so it might as well be a computer.

On the other hand, in addition to using the SEAC to test out new and advanced equipment, the SEAC is itself continually testing the components which go to make it up, and these components have been selected to give information of interest to computer design. For instance, the decision was deliberately made to use as the major vacuum tube one on which relatively little experience was available, but which had been partly designed with computer use in mind. It is this sort of experience—experience in the operation of the computer itself—which I wish to describe here.

Over-all Performance

First I would like to mention the over-all performance that has been observed. This is not too easy a thing to express in quantitative form, since some numbers that might be assigned would give a very misleading impression of the usefulness of a computing installation. To show how this could be, imagine a computer which is working at a megacycle rate, but loses just one pulse every second. Then this computer would be making errors only 0.0001 per cent of the time but it would be almost completely useless for problem solution since there would never be more than a second's continuous good operating time. We have attempted to avoid this situation by using a definition of good operation which depends on the amount of useful work performed. Thus we call "bad" time for the computer the total time which it is estimated was lost as a result of computer malfunction. Thus it sometimes comes about that the computer will make an error at a time which invalidates previous good operation which may have extended for one or several hours, and in order to make further progress on the problem it is necessary to repeat this previous work in order to recover the lost information. With the definition we use, all of this time used in rerunning the problem is considered as "bad" time. It is obvious that the operating figure that results from this is a function not only of the computing equipment itself, but also of the type of problem which is being done, and of the skill of the problem preparer and machine operator in making provision for minimizing the effect of possible machine malfunctions. Also when errors occur during the checking of the coding of a problem, it is somewhat a matter of judgment as to just how much delay a given machine malfunction may have caused. We believe, however, that the definition which is used tends to err more on the conservative than on the optimistic side.

With these considerations in mind, then, we can turn to the experience for the past year—October 1950 through September 1951. On a weekly basis, the percentage of good time during that time of the machine which was assigned to problem solution varied from a low of 25 per cent to a high of 96 per cent, the over-all average for the year being 70 per cent. That is, if the machine had been working perfectly it would have turned out the same amount of results in 70 per cent of the time which actually was required.

However, while this sort of figure on over-all operation is of interest in connection with the efficiency of a given computing installation, it does not tell us much about the performance of the individual parts which go to make up the computer. A breakdown of the relative number of hours lost for various reasons will give something more along this line, although it is necessarily somewhat rough because many intermittent troubles have unknown causes. Of the total trouble time some 34 per cent was produced by such undetermined causes or by a variety of different reasons, each a small percentage in itself. Thirty-six per cent of the trouble time was attributed to errors in the input-output equipment, the majority of these being caused by malfunctioning of the mechanical parts of the electric typewriter used, or its associated relay and electronic circuitry. Seventeen per cent of the bad time was attributed to errors in the delay line memory—either the loss or pick-up of pulses such as might be caused by improper gain of the recirculation amplifier, but which were not attributable to any particular tube or diode circuit in the system. Only a small proportion of the errors was directly attributable to the tubes and diodes, 8 per cent for diodes, 5 per cent for tubes, and 0.5 per cent for electrical delay lines.

Tube Life

Let us look at the data that have been accumulated on tube life. The SEAC uses mainly one kind of tube, the *6AN5*; nearly 75 per cent of all the tubes in the machine are of this one kind. Half of the remaining tubes are *6AK5*, the remainder being made up of a large variety. A bit of an engineering gamble, call it calculated risk if you will, was undertaken in

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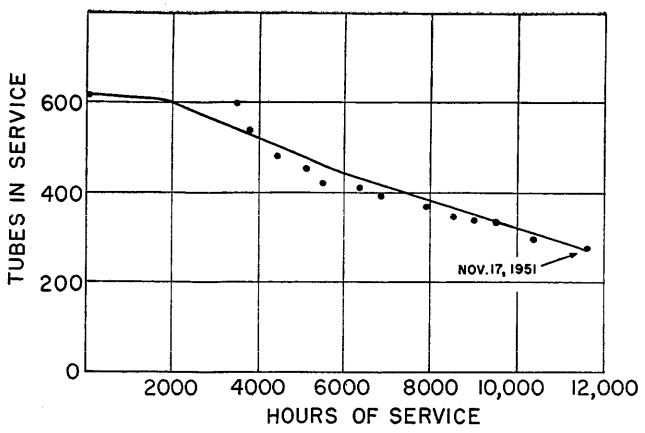

Figure 1. 6AN5 tube life in SEAC

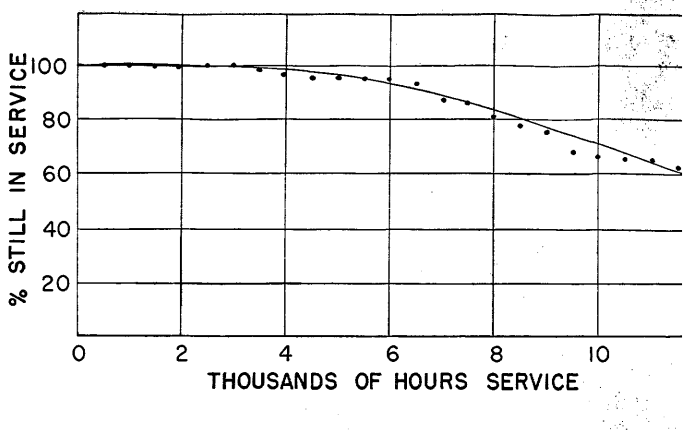

Figure 2. A history of 350 tubes in SEAC

using this *6AN5* so extensively. At the time the SEAC program was initiated, very little life experience was available on this tube, but it was selected because its characteristics had been developed partly to meet computer requirements, and in its design a great deal of attention had been put toward doing as much as was known to make a reliable tube. The tube was initially developed during the war as a high-gain broad-band intermediate frequency or video amplifier. Its characteristics looked sufficiently promising so that as part of a program of component development for the Army Ordnance Department the National Bureau of Standards sponsored further design work aimed at unusually high reliability. Care is taken in the filament construction to prevent weak spots which would be likely to open up. Passive nickel is used for the cathode to avoid interface troubles; and particular attention is paid to keeping the grids cool and preventing emission from them. The tube goes through a careful inspection procedure, and costs accordingly. These points in the design seem to have produced good results. In the SEAC operation, no attention is paid to any particular cycle for turning the filaments on or off. They are simply snapped on or off whenever desired, and yet filament failures in over 1,000 tubes are almost completely unknown. In the last year not more than two or three have been observed. Similarly there has been no evidence of cathode interface formation or trouble from grid emission.

Another design decision was that the tube would not be derated but used in the computer in such fashion that under certain combinations of circumstances the element dissipations or currents might reach those specified by the manufacturer. Actually, the circuit in which it is used is limited not by plate but by screen grid dissipation. Plate saturation takes place and the plate dissipation can only reach one-third to one-half the manufacturer's rating while the screen grid reaches the full rating. On the other hand, under certain circumstances peak currents of as much as 100 milliamperes at 50 per cent duty factor are drawn from the cathode.

Up to the present the SEAC has been in operation for somewhat over 12,000 hours, and Figure 1 shows the experience with the 600 tubes which made up the first installation. You will note that 50 per cent of them were in service slightly more than 10,000 hours. The rejections on which this curve is based are not in general for failure in service, but rather for passing our lower specification limit in routine maintenance tests. These specifications are shown in Appendix I, and are based mostly on arbitrary judgment. How this curve would be affected under changes in the specifications is not known.

Looking at the curve, you will note that there were very few failures for the first 3,500 hours, followed by a rather rapid drop-off. When we noticed this sudden drop-off, we found that due to an error some 250 of the tubes were installed such that their filament voltage was from 5 to 10 per cent higher than 6.3 volts. These tubes were failing to pass specifications rapidly at about 3,500 hours, which shows as anyone would guess that at least in this instance abnormally high filament voltage is not conducive to long life. When these abnormally run tubes are removed from the sample, the curve shown in Figure 2 is obtained. This you will see is quite a bit smoother and indicates that nearly 60 per cent of the tubes are still in operation after 12,000 hours of service. An interesting feature of this curve is that it leaves the 100 per cent line gradually and at least for the life observed here is concave downward rather than being concave upward as would be the case if the failures were purely a random phenomenon. The situation shown in the cu is very desirable for computer operat since it means that early failures are most negligible and even without test them this particular group of tubes co be depended on for the first 3,000 or 4,0 hours. If the failure of the tube wer purely random function of time, the cu would be an exponential one droppi away very quickly from the 100 per ce point, and it would require very lo average life indeed to provide similar liability during the first few thou hours of life.

Since the tube has a passive nic cathode sleeve, it of course is relativ hard to activate stably. We find that initial aging period of the order of 1 hours is essential for new tubes, since in least some cases we have observed duri aging a drop in plate current of 50 per ce during the first 10 or 20 hours, with co plete recovery at the end of 100 hours.

The general conclusion is that t *6AN5* is a very satisfactory tube f computer use. Whether derating t tube would make its life any better th what is shown from these figures I ca not say. As it stands its life is only very minor source of trouble in the co puter.

Germanium Diode Life

When we turn to look at data on ge manium diode life we find that it is little bit obscured by procurement d ficulties in the initial installation of t SEAC. At the time of the initial co struction of the SEAC our diode spec fications were less stringent than at pre ent, particularly with regard to diod whose back characteristic "creeps" "wiggles"; that is, changes either slow or rapidly during test. However, at th time we had considerable difficulty in ob taining enough diodes even of the weak

ifications to fill the machine, so we in-
ed quite a large number of diodes
ch were somewhat below the installa-
specifications we were shooting for
1 at that time. It took nearly 8,000
rs of machine operation before the
was completed of insuring that all of
diodes in the machine met our present
ification on installation. This speci-
tion is shown in Appendix II.
)uring the last 4,600 hours, while the
ifications were being tightened on the
les, some 11.5 per cent were replaced.
s of course is not a very fair figure be-
se of the change in specifications but
t least an upper bound, even if prob-
a very lax one, on what the true
ire rate would be during this time. A
ch better figure comes from the ex-
ence subsequent to the uniform in-
lation of the diodes. Here we have
ie 7,700 tests on individual diodes,
because of the sequential nature of the
tine maintenance testing we can infer
t each of these diodes passed specifica-
is at a time which averages about
)0 hours before the current series of
s. This series of tests rejected 2.2 per
t of the diodes, so we can say that of
)0 diodes that were acceptable at a
er e, 5,000 hours later 2.2 per cent
ad been rejected for failing to
ifications. I want to emphasize
in, as in case of the tube failures,
jections of the diodes were based
re to meet a quite arbitrary speci-
n and not on complete short or
circuit of the diodes. These diodes
removed during routine maintenance
ods. Actually, out of approximately
)00 diodes in the machine and over a
iod of a full year, only 20 diodes were
oved for having been found to be the
use of failures in attempts at
ing problems. All the rest were re-
ed as a part of the preventive main-
ance procedure.

eventive Maintenance

n order to clarify these figures let me
cribe the system of maintenance used
the SEAC. The machine is scheduled
the basis of 24 hours a day, seven days
eek, which is a total of 168 hours per
ek. Out of this time something like 10
20 hours are scheduled each week for
ventive maintenance. During this
ie the tubes and diodes in two or three
ssis are removed and tested individ-
ly, adjustments are made to the
chanical devices, the central clock
asing is tested, test routines are run,
l marginal testing is used. This mar-
al testing procedure is particularly
simple with the circuitry that is used. The positive pulse output of every stage in the computer appears on one winding of a pulse transformer, one side of which is returned to a bus at −10 volts. Thereafter, d-c coupling is used to the grid of any tubes which are to be activated by this pulse. Thus if this −10 volt bus is made more negative, every pulse in the computer is weakened in its action on the succeeding stage, and any which are marginally low in amplitude will produce failures. Similarly the negative outputs used to inhibit the action of gates are returned from a transformer winding to a bus at +4 volts, so raising the voltage of this bus is sufficient to induce errors in any stage which has a marginal amplitude. Thus the maintenance procedure is a combination of direct testing of components and marginal checking. We believe that in the case of the circuits that we use, both are desirable. The typical stage in the computer is operated with the vacuum tubes output limited by plate saturation. Thus as the emission of the tube deteriorates, there is for a long time almost no effect on the output pulse characteristics, and then quite suddenly the output pulse becomes unacceptable. This maintenance procedure has been quite effective in catching the components which are becoming weak and removing them during the routine maintenance period and before they have a chance to cause difficulties in the problem computations. For example, during the past year among the *6AN5* vacuum tubes, 410 have been rejected as a part of preventive maintenance, but only seven have been removed for causing trouble during scheduled problem time. This is an average of only one tube in nearly two months that definitely failed during scheduled problem times. Similarly, out of all the thousands of germanium diodes that are in the SEAC, only 20 have been removed in the last year for causing trouble during problem solutions. The great preponderance of those which have been replaced have been as a result of preventive maintenance operations.

I might discuss this question of component reliability a bit at this point. One naturally tends to assume that in order to insure reliable operation of large aggregations of tubes and germanium diodes it is necessary that each component be able to be depended on for reliable operation for a large number of thousands of hours. This, it is true, is desirable but is by no means necessary. If it is present it can result in long periods of good operation between maintenance repair activities and is the dream of every computer engineer. On the other hand, though, on the large installations where only a small fraction of the cost of operation is necessary to have maintenance personnel on hand reasonably frequently, it is only necessary that there be some reasonably simple test which will permit the removal of those elements which are likely to fail before the next maintenance period. For example, if one could predict the future operation of a computer component for no more than half a day but it only took a few minutes of diagnostic test to locate those components prone to failure in the next half day, it would be entirely reasonable to do this diagnostic test procedure a couple of times a day, and the over-all problem-solving performance of the computer would be entirely satisfactory.

This is another way of saying that what we need for reliable computer performance is primarily predictably low failure rates for a given period of time. If the failure is unpredictable, it is necessary that the failure rate be very low to permit reliable operation. For instance, it would make only a very modest difference to the operating cost of a large computer if every tube in it had to be changed after 1,000 hours, provided good operation is guaranteed for this time. As another example, a vacuum tube which fails due to gradually decreasing emission can easily be detected by preventive maintenance and removed before it causes any unreliability. On the other hand, a vacuum tube which fails by a sudden short circuit or by a suddenly open-circuited filament is difficult to live with.

This desirable predictability of performance has definitely been shown by the diodes used and by the *6AN5* tubes. It is a very startling fact that so few tubes and diodes have visibly failed during scheduled computations—only seven tubes and 20 diodes in a year's operation. This leads a computer designer to look forward to the time, maybe not this year or next, but eventually, when equipment of this degree of complexity can be so designed that an over-all operating rate of 70 per cent would be considered to be grossly inefficient.

Appendix I. 6AN5 Test Specifications in SEAC

The *6AN5*'s used in SEAC are tested as follows, with 60 volts on plate and screen:

1. I_p is read with 6.3 volts on the filament with
   (A) Grid grounded
   (B) Grid at −5.7 volts

2. I_p is read with 5.7 volts on the filament with

(A) Grid grounded

(B) Grid at −5.7 volts

The tube is rejected if any one of the following conditions apply:

Reading 1(A) is under 25 milliamperes or over 55 millamperes.

Reading 1(B) is greater than 8 milliamperes.

Reading 2(A) is less than 75 per cent of 1(A).

Reading 2(A) is less than 25 milliamperes and also is less than 85 per cent of 1(A).

Appendix II. Diode Test Specifications in SEAC

All diodes are tested before clustering and again before installation in the machine.

All diodes are kept under test for at least 0.5 minute on both the forward- and back-current test, and the readings are taken at the end of that period.

A "creeper" is a diode whose back current is not steady, but tends to drift in either direction. Such a diode is acceptable only if its back current drifts less than 50 microamperes in 0.5 minute and is stable at the end of that period within the below specifications.

A "wiggler" is a diode whose back current is not steady, but tends to vary suddenly about some particular point. A "wiggler" is acceptable only if the total back current variation is less than 10 microamperes and is within the below specifications for a normal diode.

Acceptance specifications are given in the following table:

At least 100 diodes of each shipment received are tested at both room temperature and 50 degrees centigrade, and the data recorded for each individual diode. The remainder of the diodes are tested first at room temperature and to the room temperature specifications. The ones which pass this test are accepted without further testing, but the diodes which fail the room temperature test are tested again at 50 degrees centigrade for possible acceptance. These diodes are left in the oven for at least two hours at 50 degrees centigrade before readings are taken. Any diodes which fail both the room temperature and the 50-degree centigrade test are absolute rejects.

	Maximum I_b at 40 Volts		Maximum E_f at 20 Ma
	Normal	Creeper	
Before Clustering	150 μa at room temp. 250 μa at 50°C	100 μa at room temp. 150 μa at 50°C	2.0 volts
Before Installation	200 μa at room temp. 300 μa at 50°C	150 μa at room temp. 200 μa at 50°C	2.0 volts
In Service	400 μa at room temp. 750 μa at 50°C	250 μa at room temp. 500 μa at 50°C	2.3 volts

Joint Discussion*

J. Naines (Northwestern University): Mr. Slutz, would you please explain what you mean by creeper failure with diodes?

R. J. Slutz: When you put a diode on a test to watch its specifications, you observe that a sizable percentage of the diodes do not have a steady back current. For instance, our particular test is made at 40 volts back voltage on a diode of essentially the *1N34* characteristic (a little bit tighter here and there). You observe when you have tested a large number of diodes that quite a few of them do not come to a fixed back current when you first turn the voltage on but gradually change over a period of time. This may be for 10 seconds, it may be for a minute or, in the case of some of them we have observed, may carry on for several hours, with the back current sometimes gradually decreasing, sometimes gradually increasing, and sometimes doing both, going up for half a minute and then back down.

This kind of diode we define as a creeper, the back current showing a gradual change. We have found that there are enough of them so that to keep our machines supplied with diodes we cannot throw all of them out. Consequently, we have specifications which allow for this phenomenon, and we consider a diode acceptable for the machine if (a) the total amount of creep over the period of a minute is less than 50 microamperes and if (b) under these circumstances it passes a somewhat tighter specification than in the case of diodes which do not creep.

Similarly, you also find diodes which are what we call wigglers, in which this characteristic changes, not gradually, but very abruptly. It may just jump from one current value to another. Again we have not felt it necessary to throw all these out of our initial specification, but we do throw them out if this jumping, (not a single jump, but jump up, jump down, jump up, jump down), is more than 10 microamperes. If it is less, we are willing to accept it at the present time.

I may complete that by saying we have not thrown them out because we do not know whether they are particularly poorer in life than the others. Our system now is set up so that we can keep complete track of every one of the 15,000 diodes in the machine, each of which has a number, and every time it is tested its test is recorded against that particular diode. We hope as time goes on to get more information which will show us whether or not we really should throw out all these wigglers and creepers.

G. Hand (Technitrol Engineering Company): The question I have concerns the wide use of plug-in techniques. I would like to know if you have experienced any large failure of plugs and sockets.

R. J. Slutz: We have had a phenomenally low failure rate in plugs and sockets. The commonest plug-in arrangement actually used in the machine at the present time is the standard octal tube base and tube socket, which was chosen for availability and cost. It is an inexpensive combination to use as the standard plug-in unit for assemblies of diodes and for pulse transformers and delay lines. The failure rate of these plugs and sockets is not significant. I think since the project has started we have replaced, perhaps, three of these octal tube sockets in the entire machine.

L. F. G. Jones (Eckert-Mauchly Computer Corporation): On your *6AN5's* do you operate the heaters at reduced voltage or are they operated at exactly 6.3 volts?

R. J. Slutz: We try to operate them fairly near to 6.3 volts, although again in view of the experimental nature of the SEAC, we do not attempt to hold it too closely, as a matter of fact. The filament transformer is on the bottom of the rack and usually adjusted so that the tubes in the bottom rows are held pretty nearly at 6.3 volts. As you go up the rack, they drop down to about 6 volts, or even 5.9 at the very top. We know this and we have left it in the machine. We are keeping records on the filament voltages of the individual tubes. When a tube fails, the filament voltage at that particular socket is measured and recorded, and eventually, as data goes on, we hope to be able to break it down in accordance with filament voltage to see if we get significantly different records for tubes run at 6.3, at 6.15, and 6.0.

L. F. G. Jones: How many channels do you have on your magnetic tape?

R. J. Slutz: We have one channel on the currently used magnetic tapes, on the 0.25-inch tape, using a standard audio recording and reading head, which I believe leaves an eighth of an inch wide channel. Experience indicates that this tends to reduce the number of errors produced by dust particles getting onto the tape and from the number of flaws as compared to what you would get in very narrow channels.

A. S. Roberts (Rector, Pa.): On your plug-in components, do you replace them in the same location after testing? In other words, do they go back in the identical spot in the circuit?

R. J. Slutz: Yes.

A. S. Roberts: Does that include tubes, too?

R. J. Slutz: Yes; each tube is numbered and it goes in the same socket after testing.

J. Levy (Arlington, Va): There is an apparent plateau in the curves of tube life in the failures, which seems to be cyclic. Has there been any attempt to correlate this data? Do you correlate manufacturer's tube lots with your overhaul and inspection reports?

R. J. Slutz: You say the plateau seems to be cyclic?

J. Levy: About every three points there was a flattening and then drop, and three

* This joint discussion covers both this and the preceding paper by S. N. Alexander on The National Bureau of Standards Eastern Automatic Computer.

points later a flattening and drop–this may only be apparent–it may not be really a plateau.

R. J. Slutz: I have not felt that the details within three or four points were really reliable.

J. Levy: This may need some action by the tube manufacturer in his test program if it can be correlated with particular lots.

R. E. Wilson (Radio Corporation of America): Dr. Alexander, you explained that your pulses are distributed at low impedance. I would be interested in knowing what the pulse level is and what the maximum cross-talk level measures?

S. N. Alexander: By our definition the cross-talk level is zero, simply because it is below the clipping level. This clipping level was set by the inherent disturbance signals that occur in the germanium diode gating circuits. We found that when we had completed the design of these circuits so that they would discriminate against the inherent disturbance signals, the cross-talk from other circuits was less than these disturbance signals. It is very hard to define an impedance level in nonlinear circuits, but the average volt-ampere impedance level in SEAC is of the order of 300 ohms and the signal level of the order of 17 volts. With clamping and disconnecting circuits used throughout, the grids of the tubes simply see no signals unless the driving source can override the clamping and disconnect diodes and get above the clipping level.

I might say this is an example of the virtue of operating with telegraphy—all the old troubles of telephony technique go out the window. You have new kinds of troubles—different kinds of troubles—but you do get the advantage of zero disturbance up to a certain threshold.

J. Paivinen (Burroughs Adding Machine Company): Would you care to indicate something of the minimum performance characteristics assumed in your pulse circuit design and the possible effects on any bottomed operation that might be useable in the design of the machine with the *6AN5*.

R. J. Slutz: The *6AN5* we test for a minimum, at 60 volts on the plate and the screen, of 25 milliamperes plate current. In addition, we reject if there is a change in plate current of 25 per cent for a drop in filament voltage of 10 per cent. We also reject it if the change in plate current is 15 per cent for a drop of filament voltage of 10 per cent, and the lower of these two values of plate current is less than 25 milliamperes. The complete specifications are given in the paper.

The bottomed operation gives a uniformity of pulse output regardless of the strength of the tube. The plate current on test at 60 volts on the plate and screen may vary from 25 to 50 milliamperes, but the pulse out of that typical stage will vary at most by no more than about 5 to 10 per cent between these two tubes.

Because the tube is operating bottomed we do not attain standard plate dissipation. The limitation in dissipation is for the screen grid; the plate therefore is running cooler than the allowed manufacturer's rating. We believe that this probably gives us a trifle better life than would be the case if both the plate and screen were run at full plate dissipation.

J. F. Lash (General Motors Research Laboratory): I wonder if you could tell me approximately what is the maximum footage of magnetic tape that you run into the cells of the tape handling mechanism.

R. J. Slutz: A regular reel of tape, about 1,200 feet, is used in each bin.

Computing Machines in Aircraft Engineering

CHARLES R. STRANG

I HAVE been specifically asked to present a user's critical view of computing machinery with emphasis on its limitations.

This is an inversion of the situation in which aircraft manufacturers usually find themselves. We are normally the supplier rather than the user, and the users of our products rarely need this much encouragement to present their views of us very critically indeed.

Aircraft, like computing machines, are complicated to design and difficult to build. You will find those who struggle with aircraft design problems understanding and sympathetic with the difficulties involved in computing machine design.

We have gone far enough to see that there are special problems in making really full scale use of machine computing in our engineering work. There are marked differences between our work and the more academic or scientific applications for which many of the present machines were developed. I will try to convey an understanding of what our work is like.

Before I do make such comments as I have in mind, I should perhaps give some idea of how much of a user of computing equipment the Douglas Company has actually been, so that you may judge how to evaluate my remarks. In considering these data it should be kept in mind that we take a rather hard-boiled engineering view of our own work. We do not fancy ourselves as scientists and we do not undertake mathematical investigations for the sheer intellectual joy of doing so. Furthermore I do not wish to leave the impression that everything we do is dependent on large scale calculation. I suppose about 15 to 20 per cent our total work is mathematical in nature. Much of that work is a miscellany of casual calculations too small to benefit from high speed computing machinery. On the other hand, a great deal of our mathematical work tends to be concerned with operations that occur early in the formative stages of the design when much of what follows can only be tentative until the calculations are well advanced. Most of the remainder is concerned with formal demonstration that the design complies with all its requirements.

A few miscellaneous numbers may serve to give some idea of the scale of present-day aircraft engineering and manufacturing operations. For example, if we were to commit ourselves today to a 4-engine jet transport development program (which, incidentally, the newspapers say we should do) the cost up to first flight would not be less than $25,000,000, and probably more. The business risk involved is very much greater than that figure because competitive sales prices have to be set at a level such that a considerable number of airplanes must be sold before the break-even point is reached. As an example of engineering

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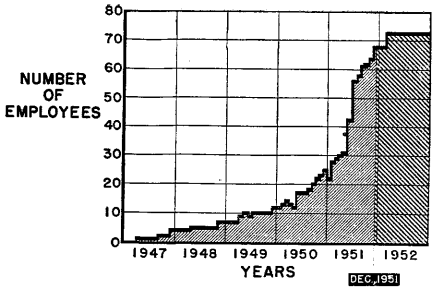

Figure 1. Growth in number of personnel needed for computing equipment

effort involved, the engineering man-hours devoted to the *DC-6* up to first flight was about 1,295,000 hours and up to now totals about 3,275,000 hours. The *DC-6* itself was a development of the *DC-4* on which engineering time totals some 3,850,000 hours. A grand total of 7,125,000 man-hours poured into the development of a specific type! There are over 250 engineering personnel working on the *DC-6* right now out of a total of something over 3,000.

Douglas Use of Computing Equipment

Against this background, Figure 1 shows the growth in number of personnel whose time was fully devoted to manipulating such computing equipment as we have had installed on our premises. It does not include the time of the engineering personnel who were the customers for the computing services and who participated in its performance. Nor does it include the staffs of outside equipment when working on our problems. Obviously, beyond this present date, we can only estimate the probable number of people whose services will be required. We have done so on the basis of the additional equipment on order and still to be received up through the end of 1952. As a parenthetical remark, the majority of these people have backgrounds in classical mathematics and physics. In the present shortage of trained engineering personnel it is important to us that computing machinery has enabled us to take real advantage of the services of a group of people whose training would otherwise have been of limited value to us.

Figure 2 shows the growth of the floor space that has had to be devoted to the installation of computing machines in our Southern California plants.

In talking about computing machines, one always seems to get around to the subject of power consumption. To remain in the tradition, Figure 3 plots the total power requirements of the various equipment as anticipated up through the end of 1952. These considerations are minor by comparison with the question of dollars involved. Figure 4 indicates the order of the direct cost in terms of actual machine cost or rental, salaries and directly chargeable items, but not including general plant overhead, as anticipated up through the end of 1952.

There has unquestionably been an appreciable dollar saving in the accomplishment of work by machine versus manual methods. This direct saving is only one

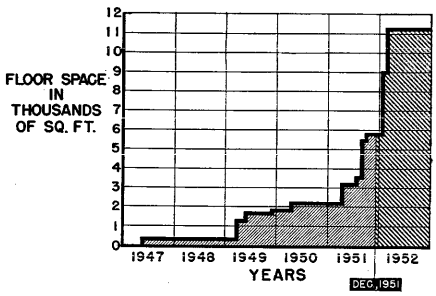

Figure 2. Growth of floor space needed for installation of computing machines in Southern California plants

of several reasons for our interest in computing machinery. As we shall see later, refined engineering design is a repetitive process. Where machine computing makes it economically feasible to accomplish a closer approach to the ideal, the value realized in terms of a better design has a magnitude hard to determine in

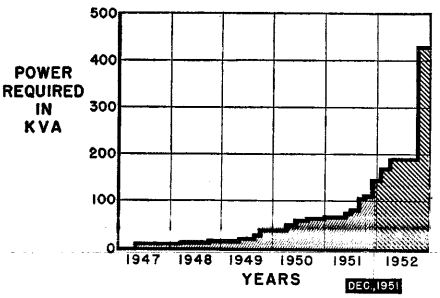

Figure 3. Total anticipated power requirements for equipment through 1952

dollars and cents. Most vital of all is the saving in elapsed time. As I mentioned previously, much of the work to be done during the formative stages of a design is only tentative. It is subject to change and deprived of final status until a large and growing volume of calculations are performed. When that work can proceed on a more firm basis, much waste of engineering time is avoided. Here a real saving is accomplished in the effectiveness of the work of hundreds of engineering personnel who may have had nothing whatever to do with the computing machines. In another sense, we are engaged in a military race. You will have to put your own dollars and cents value on winning versus losing.

Types of Machines Used

Up to this time the equipment actually installed in our plants has been a changing combination of IBM punched card tabulating machinery. However, Figures 1 through 4 reflect the fact that an electrical analogue machine of the type developed at California Institute of Technology by Dr. McCann and his associates, and being built by the William Miller Company of Pasadena under the guidance of Dr. McCann, is scheduled to go into service in January 1952. The nature of that equipment and some of the techniques developed for its use have appeared in AIEE and IRE papers by Dr. McCann.[1–3] The curves also anticipate the installation of a new Reeves Electric Analogue Computer. It is scheduled to take over in March 1952 the work that now is being done on another similar installation outside of the Douglas Company. The large jump in dollars and power consumption shown at the end of 1952 reflect the hope that at that time the two IBM Defense Calculators currently on order will be available and actually go into service. Equipment-wise this adds up, at the end of 1952, to

2 Defense Calculators (IBM)

5 Card Programmed Calculators (IBM)

1 electrical analogue (William Miller Company)

1 REAC (Reeves Instrument Company)

Miscellaneous IBM 604 electronic calculators and associated equipment

This equipment will be distributed, as our present equipment is now, among the three Douglas Company plants in the Los Angeles area.

In addition to these facilities which are operated as an integral part of our en-

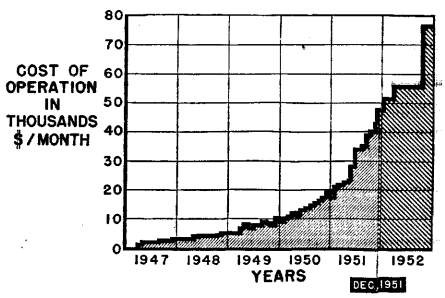

Figure 4. Cost in terms of machine cost or rental, salaries, and directly chargeable items not including plant overhead

gineering departments, we have had a number of projects which for one reason or another were carried out on various outside computing facilities. In such cases, of course, the projects were conducted largely by the staffs associated with those facilities. These have included a number of investigations, some of them extremely interesting in their nature, on the

MIT Meteor

Analogue (California Institute of Technology)

General Electric Mechanical Differential Analyzer (University of California at Los Angeles)

Thermal Analyzer (University of California at Los Angeles)

Bell Telephone Company G.P.A.C.

Project Typhoon

Project Cyclone

REAC

As a company we have designed and built several devices in the general category of computing equipment. Also, in the normal course of our work on several missile projects, we have been exposed to the computing equipment phases of the guidance systems involved.

Problems Solved

A tabulation of projects is a dull and dry way of conveying the idea of what we have been doing with these facilities, but at least it is a compact way of doing so. Figure 5 lists the projects in broad general classifications which indicate their physical nature, together with the nature of the controlling mathematical procedures involved. The list is not complete and does not by any means represent all of the applications which the total scope of our engineering work will ultimately require.

Up to this point, I have presented in a necessarily superficial way enough data to show something of the scale of our work on, and our familiarity with, computing devices. I also have indicated the rate at which that phase of our work is growing, how it compares with the total engineering operation, and something of what has so far been done with it.

To those of you to whom the scale of these operations seems large, the question will naturally arise as to what is so particularly difficult about airframe design as to really need so much engineering and computing. The answer is sardonically implied in one of our favorite definitions of our own products, which declares that an airplane is a thing that almost doesn't work—and a missile is a thing that almost does! The difficulties involved are amply attested to by the unfortunate fact that most airplane designs are failures. In our philosophy a successful airplane is one that contributes more to society than it costs. We believe that when a particular design satisfies this definition its history will be characterized by long production life, repeated reorders, and wide application. There have been thousands of different airplanes designed and built in the last 45 years and pitifully few that could be considered successful by such a standard. Furthermore the technical difficulty involved goes up by leaps and bounds with increasing flight speeds. Unhappily the cost involved goes up to some power of these complications and the penalties for inadequate or misdirected engineering effort go up accordingly.

The Engineering Method

I am aware that the more scientifically minded sometimes tend to be horrified and disappointed with us as engineers when they discover how we operate. Unfortunately the present state of the engineering art does not permit us to solve directly for a design of anything to do any stipulated job. We have to work the other way around. A design is proposed that might do the job. All our techniques are such that they pertain to the performance of the proposed design. This performance is then compared with the desired and, in general, is found wanting. The proposed design is changed, the technique applied again, and the new performance compared with the desired, and so on ad nauseum. This is true whether the problem involved is large or small. Whether it is the design of a structural member to carry a load, a supercharger vane to move enough air, or an airplane to possess a given rate of climb with one engine out, gears up, and flaps down, for example. Furthermore the total number of variables involved are so great that no one has yet proposed a computing facility that could handle them all as one problem, even if we had reached the stage where we could express them as one problem.

The user soon finds that one of his biggest problems is to develop a proper sense of proportion. He finds himself suddenly in possession of relatively tremendous mathematical power. If we are typical examples, he is intellectually unprepared for mature use of that power. The state of his art is not built on availability of such power, but on the contrary, consists of a bag of tricks to enable him to get along without it. He is hard put to direct it always either to that backlog of work he would have to do anyway by other and slower methods—or to such new applications as truly benefit his design purpose. The temptation to waste that power away on fancy business, and investigations he could well do without, is tremendous.

Digital Versus Analogue Machines

Although your interest here lies primarily in digital machines, we have found it desirable to use both physical and mathematical analogues as well as digital machines and expect to continue to use them indefinitely. As users we take a dim view of futile arguments as to the relative merits of digital versus analogue machines, or mathematical analogues versus true physical analogues. We think there is room, and need, for all. Our interests would be better served if the proponents

Figure 5. Some typical aircraft engineering problems solved using automatic computing equipment

METHOD OF SOLUTION → / DESIGN PROBLEM ↓	SIMULTANEOUS EQUATIONS	DIFFERENTIAL EQUATIONS	MATRIX ALGEBRA	HARMONIC ANALYSIS	STATISTICS & PROBABILITY	NON-LINEAR ALGEBRIC EQUATIONS
ACOUSTICAL STUDIES						
AERODYNAMIC PERFORMANCE	▒					
AERODYNAMIC STABILITY			▒			
AEROELASTIC STUDIES	▒					
AIRFOIL PRESSURE DISTRIBUTIONS						
AUTOPILOT DESIGN						
CATAPULT LAUNCH ANALYSIS						
CONTINUOUS BEAM ANALYSIS	▒		▒			
CONTROL SYSTEM TRANSFER FUNCTIONS						
FLUTTER ANALYSIS	▒		▒			
FUSELAGE & WING SECTION ANALYSES	▒		▒			
LANDING GEAR SPIN-UP ANALYSIS						
LOFTING CALCULATIONS						
MISCELLANEOUS CURVE FITTING	▒		▒			
MISCELLANEOUS DATA REDUCTION	▒				▒	
MISSILE TACTICAL EMPLOYMENT STUDIES						
RADOME DESIGN			▒			
SUPERCHARGER VANE DESIGN						
THERMODYNAMIC ANALYSIS						
TRAJECTORIES OF AIRPLANES & MISSILES						
WING SPANWISE LIFT DISTRIBUTION	▒					

of each took a generous view of the advantages of the other and tried to incorporate comparable advantages in their own design.

I have selected two particular applications to tell you about in a descriptive nontechnical way to convey to you something of the situation into which computing machinery must fit to become an integral fully effective part of an operating engineering department.

The first application selected as an example is a flutter problem. The flat plane of a wing or tail surface forced through the air edgewise wants to wave like a flag, that is, to flutter. Deflection modes of wings, fuselage, and tail surfaces may want to interact with and mutually reinforce each other. Since they are meanwhile deriving energy from the passing air stream, a sufficiently high speed will cause the oscillations to build up to the point that something fails. The mechanism is very much as if the aerodynamic forces interacting with the elastic and inertia forces within the structures had constituted themselves into a mechanical analogy of what is going on electrically in an oscillating electrical circuit. Or it could be compared to the stability of a closed loop servo system. It is our purpose as designers to keep the critical speed at which this whole process becomes catastrophic safely above any speed at which the particular airplane or missile will ever fly.

The flutter problem is one of aeronautical engineering's most difficult problems to deal with mathematically. It was one of the first on which we brought digital machine computing methods to bear. During the last six years the mathematical procedures involved have been adapted to IBM punched card tabulating and computing equipment to the point that about 90 to 95 per cent of the work is mechanized. This has benefitted us enormously at a time when much higher flight speeds and the thin airplane and missile surfaces typical of high speed design have greatly increased the probability of flutter. Our small group of flutter engineers aided by machine computing have dealt with more flutter investigations in the last few years than those engineers would normally have seen in a lifetime.

Figure 6 gives a typical formal mathematical statement of the problem. I am told that these may be described as simultaneous, 4th order, integro-partial differential equations. From the hard-boiled engineering point of view I referred to earlier, it is simpler to describe them as a mathematical mess. The airplane in question had been carried into an advanced phase of its design with some eight months of work by several hundred design personnel involved when a preliminary conventional flutter analysis indicated that the critical flutter speed was far too low. This was an unusual situation in every respect. The traditional procedure until recently would have been for the design to be completed, the prototype airplane built, and natural frequencies and modes determined by forced vibration of the prototype. Months of calculations based on these data would then be carried out. These would normally be completed at about the time the airplane was ready for actual flight. At this point it would be found that the flutter speed was not critical. No one except the flutter engineers who had been toiling industriously away in the background for months would even be aware that anybody had considered the problem. However, this particular design was progressive and far from conventional. Therefore every effort had been made to carry out a preliminary analysis, even though the work had to be based on sheer estimates of the parameters involved. To find that the design might be heir to flutter trouble this early in the game was an accomplishment in itself, but a horrible state of affairs.

To meet the emergency and supplement the usual approach it was decided to deal with the problem in all its ramifications on the analogue machine at California In-

Figure 6. Typical wing bending-torsion flutter equations

$$\frac{\partial^2}{\partial x^2}\left[EI\frac{\partial^2 y}{\partial x^2}\right]+\frac{m\partial^2 y}{\partial t^2}\pm S_\alpha\frac{\partial^2\alpha}{\partial t^2}=-\pi\rho\, b^2(x)\frac{\partial^2 y}{\partial t^2}-\pi\rho V\, b^2(x)\frac{\partial\alpha}{\partial t}-2\pi\rho V\int_0^t\phi(x,t-\tau)\left[b(x)\frac{\partial^2 y}{\partial\tau^2}+b^2(x)\frac{\partial^2\alpha}{\partial\tau^2}+Vb(x)\frac{\partial\alpha}{\partial\tau}\right]d\tau+f(x,t)$$

$$\frac{\partial}{\partial x}\left[GJ\frac{\partial\alpha}{\partial x}\right]\pm S_\alpha\frac{\partial^2 y}{\partial\tau^2}+I_\alpha\frac{\partial^2\alpha}{\partial\tau^2}=-\pi\rho\frac{b^3(x)}{2}\frac{\partial^2 y}{\partial t^2}-\pi\rho\frac{b^4(x)3}{8}\frac{\partial^2\alpha}{\partial t^2}-\pi\rho V\, b^3(x)\frac{\partial\alpha}{\partial t}+g(x,t)$$

LEGEND

- EI = BENDING RIGIDITY OF WING
- GJ = TORSIONAL RIGIDITY OF WING
- m = MASS PER UNIT LENGTH OF WING
- S_α = UNBALANCE MOMENT PER UNIT LENGTH OF WING
- I_α = MASS MOMENT OF INERTIA PER UNIT LENGTH OF WING
- ρ = DENSITY OF AIR
- $b(x)$ = SEMI-CHORD OF WING
- V = FORWARD VELOCITY OF WING
- $\phi(x,t-\tau)$ = LAG FUNCTION DESCRIBING GROWTH OF LIFT ON WING
- $f(x,t)$ = ARBITRARY FORCING FUNCTION
- $g(x,t)$ = ARBITRARY FORCING FUNCTION
- $\alpha(x)$ = ANGULAR COORDINATE DESCRIBING TORSION OF WING
- $y(x)$ = VERTICAL COORDINATE DESCRIBING VERTICAL TRANSLATION OF WING

THE EQUATIONS FOR THE MECHANICAL SYSTEM ARE SOLVED BY WRITING THEM IN THE FOLLOWING FINITE DIFFERENCE FORM, WHICH IS ALSO A SET OF EQUATIONS DESCRIBING AN ELECTRICAL NETWORK.

(1) ELASTIC

$$\frac{\partial\frac{\partial y}{\partial t}}{\partial x}\bigg|_{x=x_n+\frac{1}{2}}=\frac{\frac{\partial y}{\partial t}\big|_{n+1}-\frac{\partial y}{\partial t}\big|_n}{\Delta x_{n+\frac{1}{2}}}\qquad EI_n\frac{\partial\theta}{\partial x}\bigg|_{x=x_n}=-EI_n\frac{\int\left(\frac{\partial\theta}{\partial t}\big|_{x=n+\frac{1}{2}}-\frac{\partial\theta}{\partial t}\big|_{x=n-\frac{1}{2}}\right)dt}{\Delta x_n}$$

$$\frac{\partial M}{\partial x}\bigg|_{x=x_n+\frac{1}{2}}=\frac{M_{n+1}-M_n}{\Delta x_{n+\frac{1}{2}}}\qquad \frac{\partial Q}{\partial x}\bigg|_{x=x_n}=\frac{S_{n+\frac{1}{2}}-S_{n-\frac{1}{2}}}{\Delta x_n}$$

$$\frac{\partial\alpha}{\partial x}\bigg|_{x=x+\frac{1}{2}}=\frac{\alpha_{n+1}-\alpha_n}{\Delta x_{n+\frac{1}{2}}}\qquad \frac{\partial\alpha}{\partial x}\bigg|_{x=x_{n-\frac{1}{2}}}=\frac{\alpha_n-\alpha_{n-1}}{\Delta x_{n-\frac{1}{2}}}$$

$$\frac{\partial}{\partial x}\left(GJ\frac{\partial\alpha}{\partial x}\right)_{x=x_n}=\left[GJ_{(x_{n+\frac{1}{2}})}\frac{\int\left(\frac{\partial\alpha_{n+1}}{\partial t}-\frac{\partial\alpha_n}{\partial t}\right)dt}{\Delta x_{n+\frac{1}{2}}}+GJ_{(x_{n-\frac{1}{2}})}\frac{\int\left(\frac{\partial\alpha_{n-1}}{\partial t}-\frac{\partial\alpha_n}{\partial t}\right)dt}{\Delta x_{n-\frac{1}{2}}}\right]\frac{1}{\Delta x_n}$$

(2) MASS

- $\Delta x m_n$ = MASS OF nth CELL
- $\Delta x S_\alpha$ = UNBALANCE MOMENT OF nth CELL
- $\Delta x I_\alpha$ = MOMENT OF INERTIA OF nth CELL

(3) AERODYNAMIC APPARENT MASS COEFF.

$$\Delta x_n\pi\rho b^2(x_n),\ \Delta x_n\pi\rho b^4(x_n)\tfrac{3}{8}\ \Delta x_n\pi\frac{\rho b^3(x_n)}{2}$$

(4) AERODYNAMIC DAMPING COEFF.

$$\Delta x\pi\rho V b^2(x_n),\ \Delta x\pi\rho V b^3(x_n)$$

(5) AERODYNAMIC FORCES (CIRCULATORY)

THE INTEGRAL IN THE EQUATIONS OF MOTION MAY BE WRITTEN IN THE FOLLOWING OPERATIONAL FORM:

$$\left[\Delta x 2\pi\rho V\int_0^t\phi(x_n,t-\tau)\left(b(x_n)\frac{\partial^2 y}{\partial\tau^2}+b^2(x_n)\frac{\partial^2\alpha}{\partial\tau^2}+Vb(x_n)\frac{\partial\alpha}{\partial\tau}\right)d\tau\right]=\Delta x 2\pi\rho V\left(\phi(x_n,p)\right)\left(b(x_n)py\pm b^2(x_n)p\alpha+Vb(x_n)\alpha\right)$$

$$\left(\phi(x_n,t)\right)\cong\frac{a_1+a_2\frac{b(x_n)}{V}p}{a_3+a_4\frac{b(x_n)}{V}p}$$

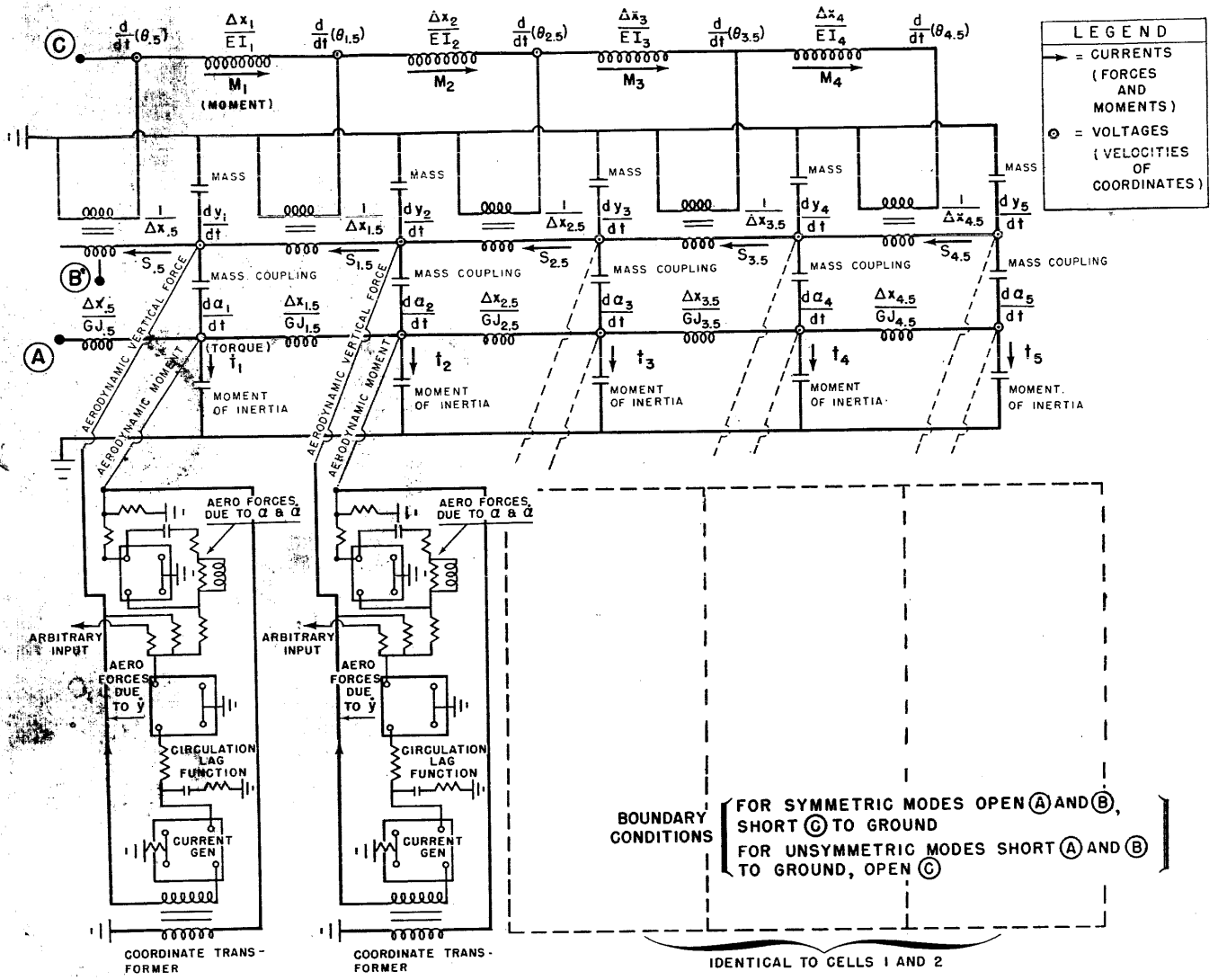

Figure 7. Circuit for typical wing bending-torsion flutter problem

stitute of Technology. It was necessary to supplement the machine with additional equipment which had to be designed for the purpose and this of course took time to do. Figure 7 indicates the general nature of the circuitry involved. During the preliminary analysis stages, the analogue confirmed the predictions of the conventional analysis that flutter was inevitable. Design changes to affect a cure were considered to the tune of 126 separate investigations of mathematical systems similar to those shown by Figure 6 except that the actual case was appreciably more complex. After design decisions based on these 126 solutions had firmed up the redesign, the nearly final version was again put back into the machine and 50 more solutions covering numerous variations were made. It was a time consuming project to carry out this enormous volume of work. It did necessitate changes in the configuration of the airplane and the addition of structural weight. This latter is a thing that an aeronautical engineer resorts to with a reluctance that is the essence of his profession. It is conceivable that the entire project might have been an utter failure without the accomplishment of the work that I have described in such an over-simplified fashion. On the other hand, while it was being accomplished the entire project was delayed to one degree or another, schedules were thrown off, costs were going up and time was going by. The management's reaction was to arrange for the construction of a similar analogue computer so that it could be brought to bear on such problems at the earliest possible moment. This is the equipment that I mentioned earlier as scheduled for completion in January 1952.

Two basic points I would like you to extract from this short story—one is the number of times that the solution had to be carried through—176 times—the other is a sense of the compulsion under which the men were working who carried out the project.

A Catapult Problem

The second case that I am about to describe is a physical system not so mysterious to deal with but equally typical of our problems. It has to do with solving the equations of motion of a catapulted airplane at the instant it is airborne. It is typical of that class of problems which are fundamentally simple but become odious mathematically when many necessary details are taken into account. When a mission requires a naval airplane operating from a carrier to take off at weights greater than it can take off under its own power, some assistance, usually in the form of a catapult, is used to attain flight speed. Conventional tail wheel airplanes rolling down the deck with the tail wheel in contact are in a tail-down high-lift attitude suitable for flight at the speeds at which they reach the take-off end of the deck. No particular problem

except the attainment of the necessary speed is involved. More modern nose-wheel type airplanes, on the contrary, reach take-off at a flatter angle, which the pilot has to correct as he leaves the deck. When nose-wheel type airplanes began to be used on carriers, the carriers had become pretty big. Flight decks were about 70 feet above the water. The pilot had about two seconds to collect his wits, get his airplane into flight attitude, and be on his way. This is obviously a pretty marginal operation, but it has been a highly successful one.

Figure 8 is a diagram of a tricycle gear airplane intended for such operations. The design was carried out, the prototype airplane was built and put through our manufacturer's flight test. It was then delivered to the Navy for continued flight testing, including simulated carrier flying. By this time production versions of the airplane were moving down the assembly line. This was the situation when it was decided that this would be the airplane on which carrier operations in bad weather and night flying, or both, should be undertaken. Now this was a horse of a different, and very dark, color. Flying off into the rain and darkness must be done on instruments. When subjected to catapulting accelerations, the instrument gyros must be caged. The pilot who in good weather day flying had two seconds to collect his wits and clear an ocean he could see 70 feet below him—now has the same two seconds to collect his wits, uncage his gyros, focus his attention on his flight instrument group—and fly off into the stormy darkness on instruments without dropping into an ocean that he can not see! It turns out, incredibly enough, that the boys can do that, too—if the airplane isn't pitching unpleasantly at the moment it is catapulted. Unhappily, the Navy flight tests showed that this was exactly what it was doing. It was absolutely necessary that some combination of dimensions and forces be found which would automatically deliver the airplane at the end of the run possessed of an angular motion that would help the pilot through his critical first two seconds.

This now brings us to our problem, and to the equations of motion given on Figure 8. These describe, simply enough, the fact that such an airplane, during the few seconds of its catapulting run and under the influence of all the forces acting during that time, tends to rock back and forth alternately between nose wheel and tail wheel. Each of these introduce forces which are functions of the load-stroke characteristics of their respective shock absorbing systems. These forces, incidentally, not only inject mathematical discontinuities but involve a hysteresis loop that is the result of the fact that the load-stroke curve is not the same when the shock strut is moving in as it is when the shock strut is moving out. In other words, these discontinuous forces are non-linear. Lift, drag, thrust, and acceleration forces are, of course, changing continuously. Taking all these mathematical horrors into account expands the simple equations of motion shown on Figure 8 into the state of affairs shown by Figure 9. These would obviously be long and arduous to solve by manual methods, as we found out when we tried to do it on a much simpler version than this.

The problem was set up for solution on an International Business Machine Card-Programmed Calculator, fortunately equipped with two storage banks. The procedures involved have been described in detail in a published paper by John Lowe,[4] who is the supervisorof Computing Engineering at the Santa Monica plant of Douglas Aircraft. Investigating the effect of changes in the location of the catapulting force, the characteristics of the shock absorbing systems, the physical location of the gears, different wind speeds over the deck, et cetera, made it necessary to carry out that procedure some 55 times. The design features that were incorporated in the airplane as a result of these calculations were checked against flight tests carried out by the Navy, and the results were in excellent agreement. The modifications to the design were successful in delivering the airplane off the deck automatically under conditions the pilots are well able to handle. In fact it was so successful that we now have to go through the whole procedure for four other airplanes! In the meantime, I think it is interesting and significant that the difficulties involved were such that we could not be assured of success. Therefore, while the calculations were being carried out, the Navy hedged its bet by paralleling our work with a flight test program to which some 50 hours of flight time were devoted. Fifty hours is a great deal of flying when you are only interested in the first few seconds of each flight. When weighing computing costs, it is fair to remember that a 50-hour flight test on this kind of equipment will buy a lot of computing machines. Now again I would like you to observe the same two basic points—the number of times that the solutions had to be carried out, and the sense of urgency under which the men worked who carried it out.

You may ask why the catapult problem was not put on the analogue. It will not be necessary even to argue the relative merits of the two types of equipment. The fact is that for the flutter job I described first we had already contracted for all the analogue time available to us. Both these problems were going on at the same time. They had two of the most powerful machines in the Los Angeles area tied up almost completely for weeks. These two problems were not even on the same airplane, and they were not the only airplanes we were working on. Hundreds of other problems were given slight treatment or none during that period.

To describe a really full-scale use of an adequate computing facility in a large engineering effort it would be necessary to multiply such situations as I have just described by perhaps several hundred times.

These are fed into the computing facility from a number of engineering specialty groups. The computing facility finds itself taking them all on at once like a master chess player playing many games simultaneously. Moving from one to another continually but returning periodically to the later developments of each problem in turn. Our operations to date are very very far from such a scale. Fortunately we have had six years to come

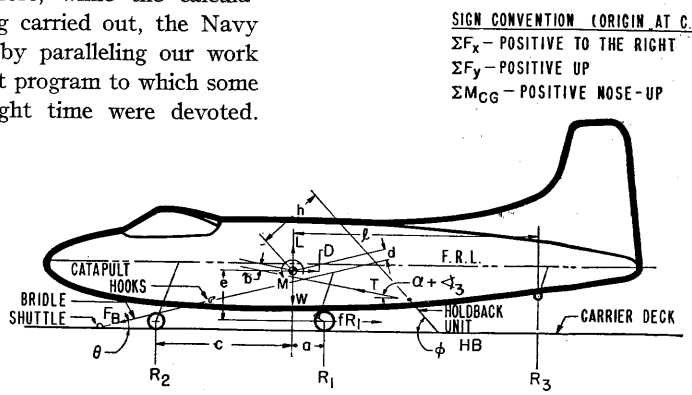

Figure 8. Catapult take-off diagram

(1) $\Sigma F_x = m\ddot{x} + fR_1 + D - T\cos(\alpha + \triangleleft_3) + HB\cos\phi - F_B\cos\theta = 0$

(2) $\Sigma F_y = R_1 + R_2 + R_3 + L + T\sin(\alpha + \triangleleft_3) - W - F_B\sin\theta - HB\sin\phi - m\ddot{Y} = 0$

(3) $\Sigma M_{CG} = bT + cR_2 + dF_B - M - \ell R_3 - aR_1 - efR_1 + h(HB) - I\ddot{\alpha} = 0$

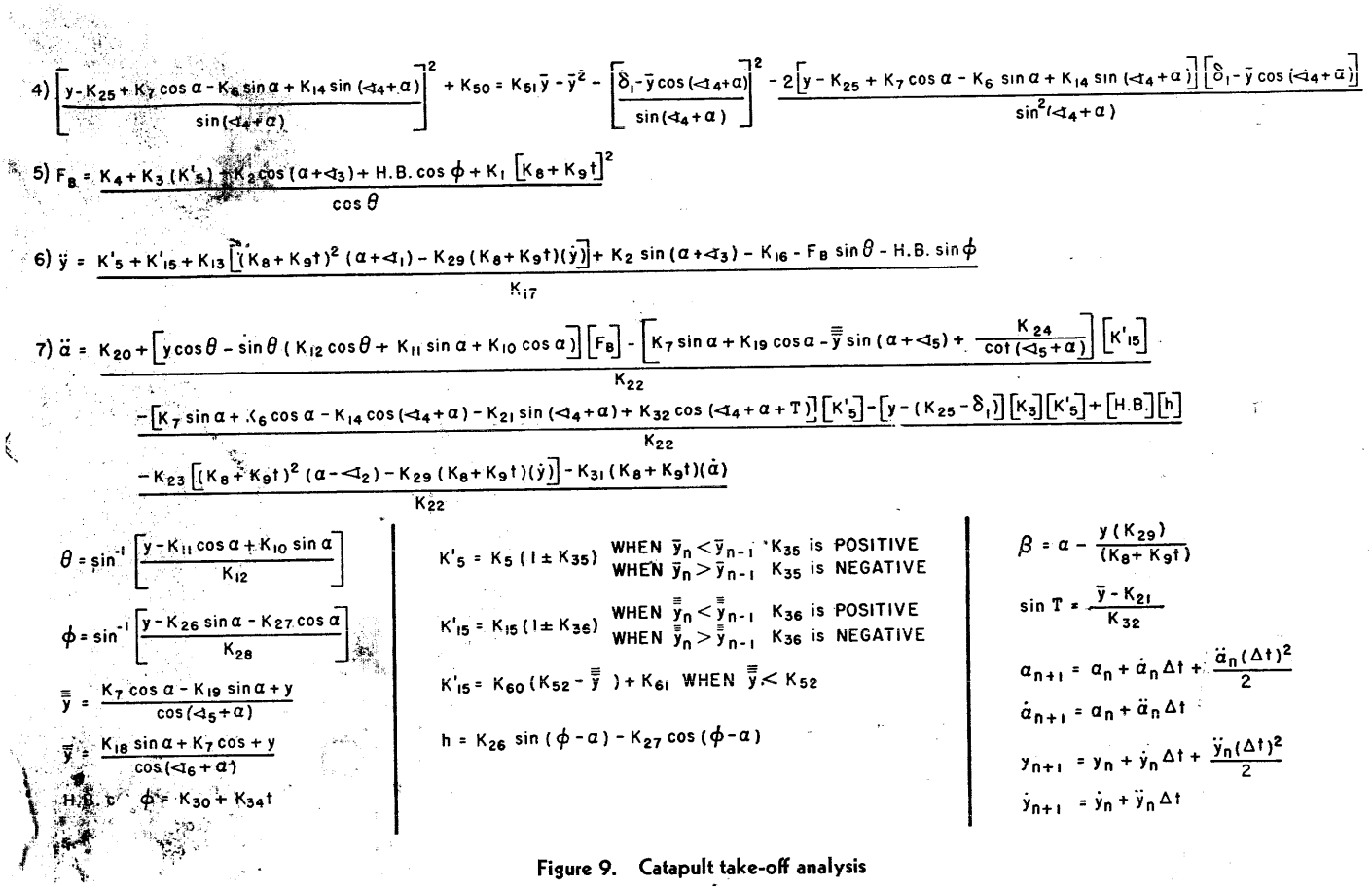

Figure 9. Catapult take-off analysis

as far as we have. I think we needed that preparation to arrive at a point where we have any hope of effectively using the relatively tremendous power of the equipment we are to start using over the next 12 months. How far that equipment will take us towards realizing such an increase in the number of problems we can deal with I cannot guess. However, I doubt very seriously whether it will make it possible to do all that we would like to be able to do. The reason for that, as you can see from what I have said, lies entirely in the fact that for some years to come our concern in realizing full utility from big machines will not be in solving a few big problems but will be in the more agile handling of enormous numbers of problems. Some of them will be larger, some smaller, than I have discussed here—but on the average of about that order.

Some Machine Design Objectives

The design of any machine is a matter of compromise and balance of its functions for the purpose intended. I am sure this balance has been earnestly sought in the design of all big computing machines. Almost everything I have said has been calculated to show the importance, to such users as ourselves, of really flexible input and output equipment.

It seems to me that most of the machines I know about are much cleverer in their internal operating philosophy than they are in their input and output devices. In our case, as we have seen, normal usage requires many repetitions of a given procedure, each time with changes in some of the initial parameters. We typically find on examination that nine times out of ten we have no further interest in the results but must try again. We must be able to completely remove the problem from and later return it to the machines at will. In such a case, obviously the design balance has to be shifted to a much heavier emphasis on the input and output equipment.

I am not saying that the input equipment and coding must be simple, though that would be nice. I am saying that it should be possible to perform those operations without tying up the computer itself.

Obviously, mechanization of the coding process by coding machines like Dr. Aiken has been developing are very much to the point. In the case of the output equipment the same sort of reasoning applies. We would not be interested in permanent records of most runs. We are interested in knowing immediately what the results have been. Some device that permits scanning of selected values from the internal storage, such as has recently been done on a display cathode-ray tube on Project Whirlwind, is excellent. Then we are in a position to examine the effects of the last change. We can either determine what to change next, or decide that we are satisfied and that we do want a permanent record. Alternatively, we can decide that we want that problem completely off the machine to take time to study what to do next. If the machine has a printer output, it should be possible to free the main machine by clearing its storage into an auxiliary storage and printing out from there. But we should ordinarily not have to do that to find out what is in the storage.

Conclusion

In conclusion, our engineering use of computing machinery has progressively increased in scope and magnitude during these past six years. At the beginning of that period we applied machine methods on a very modest scale. We did so in the hope that it would be the eventual means of breaking our major design bottleneck—the ever growing volume of mathematical investigation demanded by modern aircraft. Machine computing has been at least partially successful in accomplishing that purpose. The scale of our operations has grown naturally from its tentative beginnings to the point that machine computing is definitely

indispensable now. It is becoming increasingly vital at a startling rate.

Computing machines are themselves an engineering product. It is entirely likely that, in their ultimate development, the engineering profession itself will be the biggest user of that product.

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A Review of the Bell Laboratories' Digital Computer Developments

E. G. ANDREWS

THE Bell Telephone Laboratories have designed and built seven digital computers. They are all electro-mechanical types using telephone systems relays and teletype transmitting and recording devices as their principal apparatus elements.

This succession of developments had its origin in 1938 in the mind of Dr. George R. Stibitz, then a research mathematician with the Bell Laboratories. Stibitz observed that in one laboratories' development area, a considerable portion of computing effort involved complex number arithmetic computations. Another development area was designing dial systems using relays and crossbar switches as the principal apparatus. Stibitz recognized that the design techniques employed by this latter group were directly applicable to a systems design which could also produce a computing system for the first group. He designed such a system. He called it a "complex number computer."

Mr. Samuel B. Williams, a telephone systems design engineer, supervised the engineering and manufacturing of this early computer. It is believed that he thus became the one who first produced an automatic digital computer for purely scientific computing.

Dr. Thornton C. Fry publicized this creation before the Mathematical Society at Dartmouth in the fall of 1940.[1] Demonstration equipment consisting of a keyboard input device and a teletypewriter for recording answers was installed at the University. This equipment was connected by a telephone circuit with the computer in New York. Those attending the conference placed their own test problems on the keyboard at Hanover, N. H. The computer in New York made the computation and controlled the printing of the answer on the teletypewriter at Hanover. The complete operation required about 1 minute. This feat of remote control operation was not to be duplicated until a computer conference was held in Washington, D. C., 10 years later.

With this complex number computer as the pioneer and with the Model VI as its latest achievement, the Bell Laboratories computer development has spanned the pre-electronic computer development era. The seven computers now are known by Model numbers, with Model I being the designation of the complex number computer. Two Model V computers were built. Table I shows some statistical information about their size and use. The Models V and VI, although operating at electromechanical speed, offer several challenges to current electronic computers. While the same cannot be said of the Models I to IV, nevertheless, they have features of interest.

Model I

The Model I consisted of about 400 relays and ten crossbar switches. It was operated from any of three stations located in various parts of the Laboratories' 463 West Street building. The station equipment consisted of a number of push button keys for originating a problem and a teletypewriter for recording the answer. It is the only one of the seven computers to employ crossbar switches.

Fundamentally, the Model I could handle only two kinds of problems, multiplication and division of complex numbers. The results of successive such problems could be accumulated when the operator required it. This feature made it feasible to add and subtract complex numbers. By multiplying a number by $+1$ or -1 with the accumulator key operated, the number was added to, or subtracted from the previous accumulation.

This computer operated with binary coded decimal notation, with the decimal digits 0 to 9 being represented by the binary numbers 0011 to 1100. The input and output information consisted of eight place numbers, but the calculator carried operations out to ten places, the two extra places being used to improve accuracy when accumulating the results of several problems.

The Model I was in daily use until 1949 when it was removed from service due to obsolesence and to make way for its successor, the Model VI.

Model II

The Model II[2,3,4] was built for the National Defense Research Council and placed in operation in September 1943. It is truly a special purpose computer. Its purpose was to handle some specialized fire control computing for several months. But on the completion of this computing assignment, new problems arose. It is still in service.

It has about 440 relays. It uses paper tape input and output. It has a flexible control provided by external

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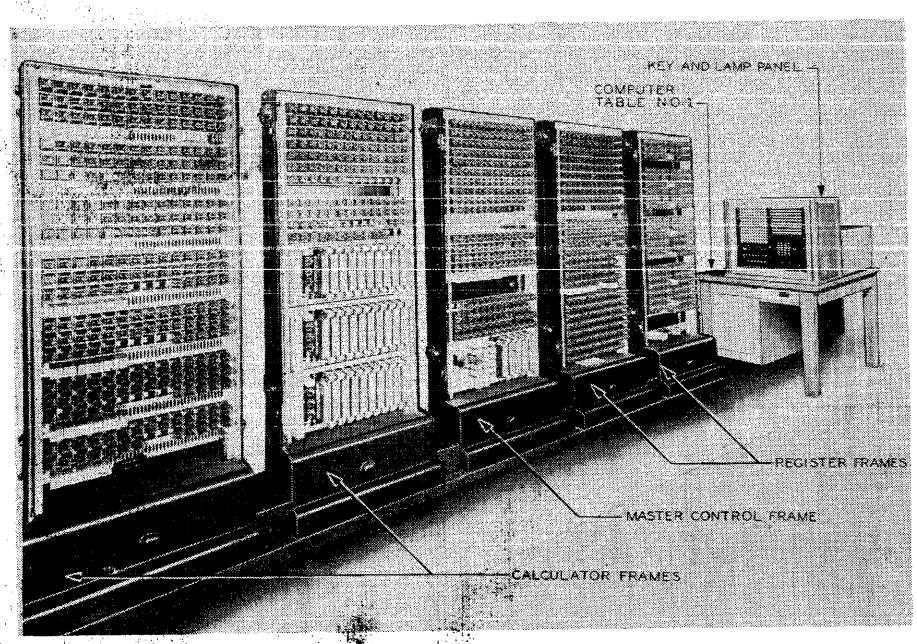

Figure 1. Model III computer. Frame equipment with covers removed

problem programming. The program is perforated on a tape which is made into a loop. The control unit recognizes 31 instructions which include the addresses of the registers.

The calculator and registers employ the bi-quinary number representation with its self-checking features. The Model II has had no respite. It is still in operation at the Naval Research Laboratory and is operated under the supervision of Mr. B. L. Sarahan.

Model III

The Model III[5] was built for the National Defense Research Council and placed in service in June 1944 at Camp Davis, N. C. It was designed to handle several kinds of problems concerned with the testing of fire control equipment. In this sense, it is a special purpose computer. However, it is sometimes thought of as being a general purpose computer in a limited sense because it handles many types of problems very creditably.

Figure 1 shows the computer as originally delivered. It then had about 1,400 relays and used seven pieces of teletype equipment. The control equipment (not shown) was located in an adjoining building. It was subsequently expanded as will be described later. Many features, new in the computing art, made their initial appearance in this computer. The foremost of these is the 100 per cent self-checking of all operations. Our engineers believe that they have achieved a design in the Model III and its successors, which positively stops the machine on any kind of a single failure. Most combinations of two or more simultaneous failures also stop the machine. The merits of this feature will be discussed further in the summary.

A second feature worthy of special note is the calculator. Almost single handed, Mr. E. L. Vibbard, a dial systems telephone switching development engineer designed a calculator employing the bi-quinary notation and using the multiplication table principle for multiplication and division operations. Those who are familiar with the design details of the calculators in all seven of the computers generally agree that from the viewpoint of logic of design and ease of understanding its operation, this calculator is the Bell Laboratories' best.

Other noteworthy features of the Model III are: table hunting, double entry interpolation, subscript notation (to be described), storage tape operation, and unattended operation. One part of the principal problem handled on this machine requires that a cubic be fitted to four items of empirical data. The four items are functions of four values of time, T_{-1}, T_0, T_{+1} and T_{+2}. With the value T_0 calculated, the Model III readily obtains the data corresponding to the four subscript values. Only the Models III and IV have this feature.

When the Army Field Forces Board Number 4 moved from Camp Davis to Fort Bliss, Tex., they took the Model III with them. In 1949 extensive changes were made to increase its general usefulness by increasing the storage capacity and adding more flexibility to the programming provisions. This computer has been in constant use. It is being operated under the supervision of Mr. Nelson E. Sowers.

Model IV

The Model IV[6] computer was built for Naval Ordnance to do the same kind of computing as the Model III. In its general appearance, it differs little from the Model III, but some changes were necessary to enable the Model IV to cope with trigonometric functions of angles from -90 degrees to $+360$ degrees. In Naval circles, this computer is known as the MARK 22 computer. It was placed in service at the Naval Research Laboratory in March 1945 and has been in constant use. Like the Model II, it is operated under the supervision of Mr. B. L. Sarahan.

Model V

The Model V[7–11] is the Laboratories' most ambitious computer development from the viewpoint of size and general flexibility. Two have been built, one delivered in December 1946 to the National Advisory Committee on Aeronautics (NACA) at Langley Field, Va., and the other delivered in August 1947 to the Ballistic Research Laboratory at Aberdeen, Md. Each has approximately 9,000 relays and 55 pieces of teletype equipment.

The Model V embraces a system of computers which can be operated together or independently. The system permits six computers and ten problem positions. As one computer completes the problem on its associated problem position it automatically picks up a waiting problem position. This arrangement makes it possible to load new problems on idle problem positions thereby providing uninterrupted use of the computing equipment itself. Thus computer Number 3, for example, may complete its solution of a differential equation set up on problem position Number 5, and in a fraction of a second start a radically different problem set up on problem position Number 2. The two installations each have two computers with 3 and 4 problem positions. Figures 2 and 3 show the Aberdeen installation.

A problem position has these facilities: one tape reader for problem input data, one to five tape readers for the program of instructions, and as many as six tape readers for tabular data. The five program tape readers allow considerable flexibility in introducing subroutines. The six table tape readers allow for extensive use of tabular data. These

Table I. Statistical Information About Bell Laboratories Computers, Models I to VI

	Model I	Model II	Model III	Model III*	Model IV	Model V	Model VI
Logical Design Features							
No. of built-in routines	2	0	0	0	0	4	200
Decimal point: fixed, or Fl.	Fix	Fix	Fix	Fix	Fix	Fl.	Fl.
Discriminating action	None	Note 1	Note 1	Note 1	Note 1	Exten.	Yes
Multiplication	Yes	Note 2	Yes	Yes	Yes	Yes	Yes
Division	Yes	No	Yes	Yes	Yes	Yes	Yes
Square Root	No	No	No	No	No	Yes	Yes
Indeterminate arithmetic	No	No	No	No	No	Yes	Yes
Special trigonometric features	No	No	Note 1	Note 1	Note 1	Yes	No
Special logarithmic features	No	No	No	No	No	Yes	No
Round off—auto. or program	No	Pro.	Pro.	Pro.	Pro.	Auto.	Auto.
Subscript knowledge	No	No	Yes	Yes	Yes	No	No
Number of addresses in code	1	1	1 or 2	1 or 2	1 or 2	3	3
Self checking	No	90%	100%	99%	100%	100%	100%
Physical Design Features							
Number of relays	425	440	1,400		1,425	9,000	4,600
Pieces of teletype equip.	4	5	7		7	55	16
No. of number registers	4	7	10	14	10	15	12
No. of digits per number	8	2 to 5	1 to 6	1 to 6	1 to 6	1 to 7	3, 6, 10
Multiplication time in sec. per 5 digit number			1	1	1	0.8	0.8
No. of problem stations	3	1	1	1	1	3 & 4	2
Arranged for unattended oper.	No	No	Yes	Yes	Yes	Yes	Yes
Number notation with self-checking: bi-quinary	No	Yes	Yes	Yes	Yes	Yes	Yes
Number notation with self-checking: "2 out of 5"	No	No	Yes	Yes	Yes	No	No
Number notation with self-checking: "3 out of 5"	No	Yes	Yes	Yes	Yes	Yes	Yes

* This column applies to the Model III after its modification in 1949.

Note 1. Very limited application.

Note 2. With multiplier specified in program.

readers are not used for tables of logarithms (base 10), antilogarithms, sines, cosines, and antitangents because these functions are wired into the machine on a permanent basis.

The calculator has these features: floating decimal point, multiplication by "short-cut" addition, automatic round off (but subject to cancellation), and indeterminate arithmetic operations. Other new features in the Model V are: special facilities for trigonometric and logarithmic calculations, rather elaborate discriminatory controls, and special auxiliary equipment for processing of various paper tapes.

The out-of-service time for the Model V computer is very low. Recent reports from the NACA installation show that their computer is turning out better than 22 hours of computing per day. It is operated around the clock; 16 hours on an attended basis and 8 hours unattended. It is operated under the supervision of Mr. Thomas B. Andrews.

Model VI

The Model VI[12,13] shown in Figure 4 was built for the Laboratories' own use. Extensive test usage on actual problems began in 1949. Incident to this, details of the final design were evolved. The computer was finally placed in regular service in November 1950. It resembles the Model V in many respects but it is somewhat simpler in design in these respects: one computer (instead of two or more) constitutes the installation, less elaborate discriminatory controls, and less elaborate problem positions. However, it has features not found in its predecessors. It has three storage tapes, one of which may have either or both numbers and instructions. Also, it has a system of several hundred semipermanent subroutines which has brought about a marked reduction in programming effort. Its value is best shown by the fact that only one set of programming instructions is required for a particular type of a problem, such as a problem of determining the frequency response for a communications system network. No further programming is required even though one problem of the type may have only six or eight parameters in simple impedance configurations while the next one may have over a hundred parameters in complex impedance configurations. In each case the internal subroutine control adjusts itself to the particular problem at hand. More detailed information about this feature has been covered in other papers.

Another feature, also contributing to a reduction of programming effort, is what has been called the "end of numbers" check signal. It is easiest explained by showing its application in a matrix problem. The problem data, in this case, includes this check signal after the last term of each line of coefficients of the matrix. The program is made applicable to a matrix of any order. Furthermore, the program is made to recognize the check signal as an indication that there are

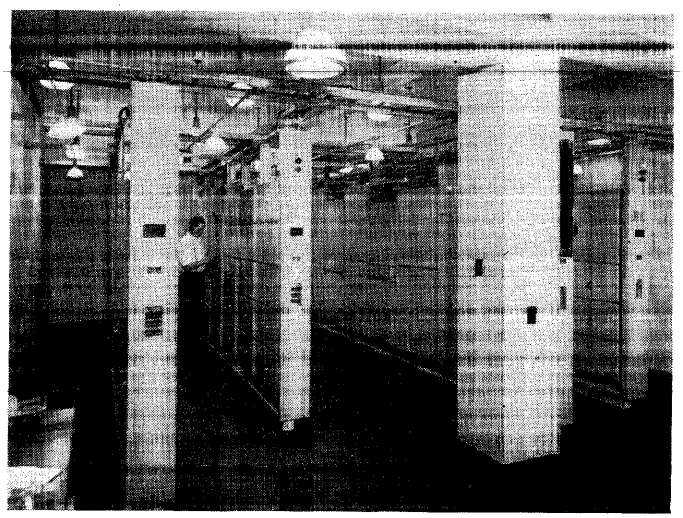

Figure 2. Model V computer. Frame equipment at Aberdeen installation

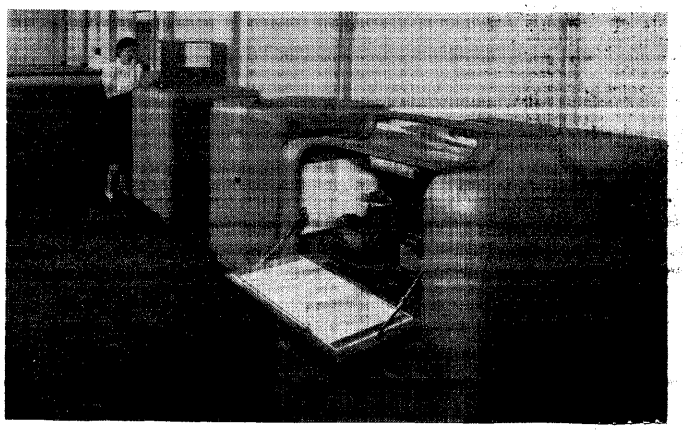

Figure 3. Model V computer. Operating room equipment at Aberdeen installation

no more coefficients for the line being processed. Heretofore, it has been necessary either to program for a matrix of a specific size or to include in the program a set of instructions for counting off a prescribed number of coefficients.

The Model VI has an automatic second trial feature which is operative under most machine trouble conditions. This feature functions only during unattended hours and obviously results in an improvement in unattended operation. This computer is operated under the supervision of Mr. D. T. Bell.

Summary

The Bell Laboratories' computers divide easily into two groups, the first including the Models I to IV, and the second including the Models V and VI. From the viewpoint of the current state of the design art, the first group belongs to an era that is past, and the second group to the era which bridges the past with the introduction of successful electronic computers. It is therefore to be expected that the Models V and VI would represent a highly satisfactory state of the development using electromagnetic apparatus. Similarly, it would be expected that they cannot be compared favorably with respect to speed or with the large amount of high speed storage capacity of the electronic type. But there are other figures of merit for gauging the satisfactoriness of a computer, and the Models V and VI possess many of them. Five of these will be discussed.

Dependability

The basic design of the control components has the heritage of the extensive experience derived from the design of telephone switching systems. Only timeproved dependable apparatus is employed, notably, the heavy duty *U* type relay. Relay contact design and detailed consideration of contact protection against electrical erosion have brought about excellent results in relay operation performance.

Ease of Maintenance

There are several factors which contribute to this feature. Generous use of indicating signals at a control panel assist in the analyzing of machine stoppages. Almost all machine failures stop the computer at once. This together with the helpful indicating signals indirectly prescribe the qualifications of the maintenance personnel. Engineering talent is not required. In fact all of the machines are being maintained by craftsmen having the same kind of training and skills that telephone systems switchmen possess.

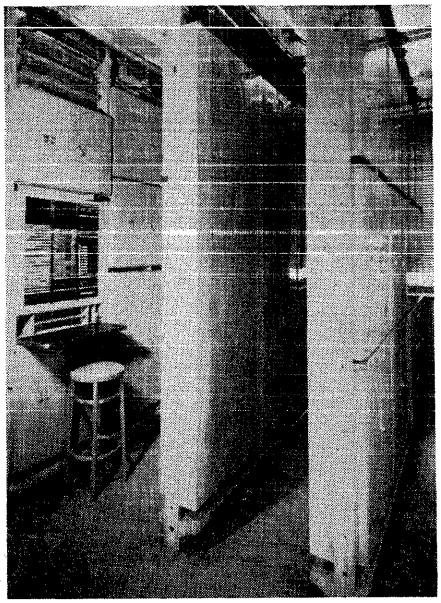

Figure 4. Model VI computer. Frame equipment

Ease of Operation

This is manifested when loading the machine with a new problem, when handling machine stoppages, when operating on an unattended basis, and when handling the transfer from one problem to another. No more than 5 minutes is required to load the most complex problem on the Model V. Even less time is required for the Model VI unless changes and additions are required in the internal routines. The Model V, if directed in the program, checks that all of the various tapes are loaded in the proper tape readers.

Because machine failures usually stop the computer at the instant of failure and because of the extensive use of indicating signals as referred to above, the amount of "down time" due to faulty machine operation is very low. Report from the two Model V installations indicate that on the average, only 15 to 20 minutes is required to locate the cause of a trouble and to take the necessary corrective action. There are two special features that are operative during unattended hours. One of these is the automatic second trial of the Model VI mentioned previously. The other is an automatic recycle when faulty operation is detected. This feature, which appears in all computers starting with the Model III, causes the control to abandon the problem at hand and to advance to a waiting problem. This feature has made unattended operation highly profitable. As stated above, the Model V at the NACA laboratories is attended on two of the three shifts. All other machines are attended on only one shift but they are all operated on a 24-hour-a-day basis.

When a computer has completed a problem, it automatically advances to pick up any waiting problem. This, too, makes unattended operation feasible.

Besides these advantages in operation ease, another has been developed but it has not yet been incorporated into any computer as far as is known. This is the self-correcting code for numerical data. Dr. R. W. Hamming devised this principle of coding.[14] A computer with this feature would show an unattended operation performance superior to anything we know today.

Ease of Programming

The Model V compares very favorably with other computers with respect to ease of programming. However, the Model VI has programming features which have brought about a marked reduction of effort compared with the Model V. The above description of the Model VI mentions the ease of programming a network problem. In such a case the programming of another network problem consists of two steps; first, prescribe the formula number, such as *A14*, for the network problem, and second, set down the parameters of the problem in accordance with the general framework of the program that was established for the first network problem. In setting down the parameters for any one of the several branches of a network, an identifying number accompanies the numerical values. For example, suppose that a branch has nine elements, consisting of three parallel circuits of a resistor, capacitor, and inductor in series. An identifying number, such as *C31*, would indicate to the control that the nine numbers which follow on the tape apply to the parallel-series configuration just described. The number *C32* might denote some other kind of a branch having nine elements, and *C33* might denote a branch having only four elements.

Similarly formula number *A15* might denote the internal program for solving a polynomial of any order up to 20. *A16* might denote the program for inverting a matrix of any order up to 12.

This feature is of prime value when there are problems having some repetitive subroutines. In these cases, the Model VI programming effort is near the minimum.

Machine Accuracy

This means 100 per cent self checking. The users of the Bell Laboratories' machines have reported only two occurrences of machine faults that resulted in machine errors. These were both reported by the NACA laboratory. No details have been received about these two cases, and as yet, no analysis is being made of them. Rather than try to disprove the claims for these two errors, it may be better to let them stay on the performance record. Perhaps more credence is accorded to our claims for self checking with two errors on the record rather than none. Because of this fine performance, the scientist uses the results obtained from these Bell Laboratories' computers with complete assurance because he confidently believes that his computer has not deceived him.

To acknowledge the names of all of those who have participated in this computer development would make a long list. It is sufficient to say that at various times, 20 engineers in the telephone switching development department have taken part in the development and construction programs. In the planning stages, mathematicians and scientists in the research department joined in the numerous discussions on fundamentals and objectives.

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The Transistor as a Digital Computer Component

J. H. FELKER

DIGITAL computers have been defined as machines that use a language explicitly and one may think of them as carrying on interior dialogues. This concept helps to illustrate one difference between the modern computer and other electronic machinery. The principal function of most electronic apparatus is to take low level signals and raise them to a power level sufficient to drive some device such as a loud speaker, servo motor, relay, or perhaps a cathode-ray tube. In a digital computer, however, there may be a thousand active elements that merely converse with one another. There may be a million alterations of state before an output device has to be energized. These internal operations need not be carried out at any particular power level. It is only necessary for one device to talk loud enough for the next device to recognize what was said. Devices are needed which have stable states that can be changed by very low input signal power. As the computer art advances, one hopes it will move towards the use of devices that listen intently rather than speak loudly. It is in this direction that the transistor can make its earliest contribution to the digital computer field.

Computer Functions

As is well known, computer operations can be divided into the two classes, memory and logic. Memory can be defined as a representation in space of a function of time. The logic operations can be defined as the recognition of spatial distributions of voltages and currents. These logic operations can be performed with passive nonlinearities, that is, a 3-terminal *and* circuit and other such logic circuits can be built with crystal diodes without the use of active elements.[1] It is necessary to use active elements only as amplifiers to make up for loss in these logic circuits and in delay lines. When the work described herein was started, it seemed that transistors could be got into digital computers at the earliest date if the transistors were asked to provide only gain and all the logic functions were performed in diode circuits while the memory functions were performed by use of delay line storage cells. This, of course, is the philosophy that was followed earlier by the SEAC group[2] with the exception that they used a vacuum-tube amplifier rather than a transistor amplifier. Since the transistor itself has voltage and current relationships quite similar to a germanium diode, it is expected that the germanium diode in a transistor computer will operate in a more natural environment than in a vacuum-tube computer and will respond to such favorable conditions by exhibiting longer life and more reliable operation than it has sometimes done in the past.

Reliability

Many earnest seekers have attempted to find out what kind of reliability can be

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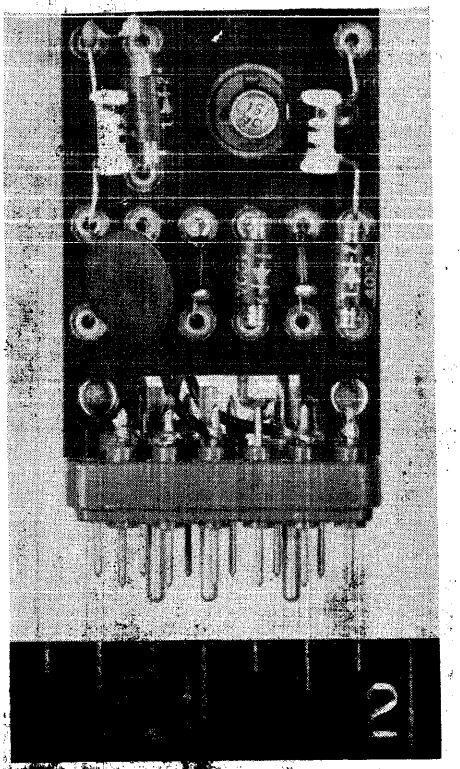


Figure 1. Packaged pulse amplifier

expect d in transistors. The answers that they obtained seem to stem as much from the inquirer's pessimism or optimism as from the facts of the case. This is because there have not been many facts established and the reliability tests that have been performed simply have not been on large enough samples nor have they been carried out over a long enough period of time to prove decisively what the reliability of transistors will be. This is not the result of negligence upon anyone's part but stems from the fact that the transistor is only 3 years old. Reliability estimates are complicated by the fact that the transistors that were put on life test as recently as a year ago are known to be very inferior to the transistors that can be made today. One figure that is indicative of the kind of life we may expect is that life figures of 70,000 hours have been predicted on the basis of 25,000-hour tests for devices that were made several years ago. It should be understood that the transistors for which this prediction was made are not the modern transistors we would use in a high-speed digital computer nor were the failure criterion used in the test necessarily the ones that would apply for use in a digital computer. It seems reasonable to say that in its relatively undeveloped state, the transistor appears to have a life that is equal to or better than the best vacuum tubes that have been made for digital computer use. Because transistors operate at reduced power levels the ambient temperature is expected to be lower in transistor computers. Resistors and condensers will operate at lower voltages and currents as well as temperatures and longer life is expected. The low voltage at which transistors operate is expected to improve the life of associated semiconductor diodes by a considerable factor.

Besides the reliability, and the power level, the speed of operation is also of interest to the computer designer. When comparing transistors to vacuum tubes one is used to thinking of the transistor as a relatively slow device. This is because vacuum tubes can be made to oscillate at 1,000 megacycles or above while transistors cannot. However, the highest frequency of steady-state oscillation is not a satisfactory criterion for the success of a device in a computer. A good vacuum tube may not have serious transit time limits upon its use at frequencies below 1,000 megacycles but the parasitic impedances of the same vacuum tube will limit its use in wide band circuits to band widths of about 20 megacycles. High-speed transistors are, at the present time, limited by transit time considerations to frequencies below about 50 megacycles but the parasitic limits are at frequencies above the transit time limitation. For that reason, the slow hole and electron of transistor electronics may be a better carrier for the production or regeneration of high speed pulses than is the much faster electron of vacuum tube electronics. This is a factor which is expected to grow in importance as transistors are improved. At the present time, transistors are entirely practical for the regeneration of pulses at a megacycle rate and rates of perhaps five times as much could be attempted with reasonable hope of success. This puts the transistor in a competitive position with vacuum tubes insofar as speed is concerned.

Completed Components

One of the first transistor computer efforts has been the development of the high-speed regenerative amplifier shown in Figure 1. This amplifier operates from a maximum supply voltage of −8 volts. The total power drain of the amplifier is approximately 50 milliwatts. When triggered by an input pulse of 2 volts and a current of 0.75 milliampere this amplifier will develop a 5-volt 10-milliampere output pulse. The input pulse need last for only a 0.1 microsecond and the output pulse will be a 0.5 microsecond pulse whose duration and time position is set by a master clock signal rather than the input pulse. The amplifier is, therefore, an almost ideal amplifier for use in serial computers. The package illustrated was designed to use the plug-in type transistor. Recent attempts to miniaturize the amplifier by using the bead version of the transistor have resulted in the package shown in Figure 2. Using the first package, a binary word generator, a serial adder, delay line storage cells, and a complete 16-digit serial multiplier have been built. The multiplier uses 42 transistors and operates on a total power supply of less than 5 watts. It occupies almost half of a standard relay rack. It is believed that the entire multiplier could be put in about one-third of an ordinary shoe box. To do this, it would be necessary to package the logic circuits as well as the transistor amplifier. It should be pointed out that the most encouraging thing about miniaturizing transistor systems is not so much the small size of the transistor but is the extremely small amount of power that has to be dissipated in the system.

Regenerative Amplifier

Some circuit considerations may be of interest at this point. Transistor circuit work is handicapped because some of the working concepts that have enabled engineers to turn out vacuum-tube circuits so successfully in the past do not provide the same assistance in transistor design work. In the first place, the input impedance of a vacuum tube is almost infinite, or at least positive. The input impedance of a transistor is more apt to resemble a short circuit than an open circuit and cannot always be relied upon to be positive. In fact, in computer work it proved so difficult to develop high-speed circuits in which the transistor input impedance was positive that almost all

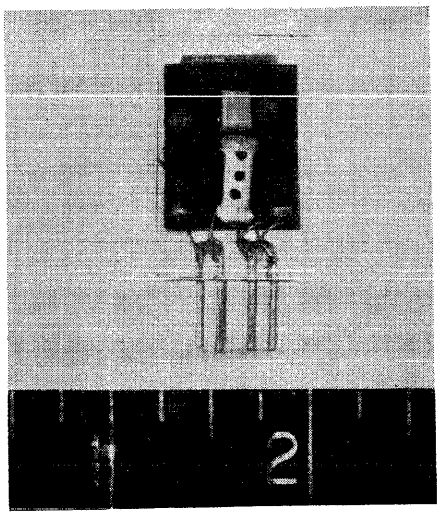


Figure 2. Miniaturized pulse amplifier

workers in the field have decided to live with the negative input impedance and exploit it rather than try to suppress it. Then too, the difficulty of working into a short circuit has proved to be a considerable psychological handicap. However, most workers in the field now consider that a short circuit is just as respectable an input impedance as an open circuit is. In Figure 3, the input characteristic of a diode is illustrated. When the bias is negative the input impedance is very high and when the bias is positive the input impedance is very low. The input characteristic of some transistors follows the same general form. The transistors made for high-speed applications, however, have the type of characteristic shown in Figure 3. If the voltage at the emitter is first negative and then raised towards ground, the emitter current will be very small and of the same order as the reverse current of a diode. As the voltage is raised, a point will be reached at which the input impedance becomes negative. This point is called the peak point. The point on the characteristic at which the impedance ceases to be negative is called the valley point. This characteristic has been exploited in the circuit shown in Figure 4. The circuit is arranged so that without a transistor present, current will flow through *R1* and diodes *X1* and *X2* to hold the junction of diodes *X1* and *X2* at a voltage just below the peak point of the transistor. When a transistor is inserted the emitter current taken will be very low. Now if the input lead is raised above the peak point, the emitter will be raised in voltage to its negative resistance region. If the transistor has sufficient band width it will not be stable on the negative resistance portion of its characteristic and will snap out on a load line provided by the stray capacity of the circuit to a point *D* illustrated in the figure. The capacity will then discharge from *D* to *B* at which point diode *X2* will conduct and the transistor will be locked up in its high current state. Once the emitter starts to go negative diode *X1* cuts off and the driving source is isolated from the emitter. What has been described is a flip-flop rather than an amplifier. However, by supplying a regular succession of reset pulses to the base of the transistor, the circuit can be made to behave as a pulse regenerator, that is, every time an input signal locks the transistor in its high current state the next positive pulse that comes to the base will reset the transistor to its low current state.

The circuit has been used with a reset pulse consisting of a 1-megacycle sine-wave signal from a master clock. The diode *X3* permits only the positive halves of the sine-wave to appear at the base. If the transistor has not been locked up in its high current state by an input signal, the base pulse will have no effect on the transistor. However, if the transistor is locked up at *B* the positive base pulse in effect pushes the emitter voltage down towards *C*. When the negative resistance region is reached at *C*, the emitter snaps over to the high impedance portion of its characteristic and the stray capacities charge back to point *A* where the circuit rests as it awaits another trigger. If the signal arrives just before the clock lets the base voltage reach ground, the transistor will trigger when the clock signal goes through ground and the onset and the end of the square wave output will be determined by the clock rather than the input, provided only that there is an input. Since the input voltage must raise the emitter only from point *A* to above the peak point, little voltage is required to trigger the transistor. An output voltage of 4 to 6 volts is obtained at the collector. The input current need be only slightly greater than the current that flows through *X1* into *R2* when the circuit is in the quiescent state. In the circuit shown the required input current is about 0.75 milliampere while the resulting collector current is of the order of 10 milliamperes. As transistors are made with peak points that are more uniform, the point *A* can be brought closer to ground and the triggering voltage can be reduced. The present practice is to bias *X2* at -1 volt and supply a trigger of about 1.50 volts. This means that the only requirement on the transistor peak point is that it lie between -1 and $+0.5$ volts. It is believed that a bias on *X2* can be chosen that will make the circuit extremely reliable. Experience indicates that obtaining reliability from transistors is by and large a matter of designing circuits that allow sufficient margin for such variables as the peak point.

Uses of Amplifier

The nature of the input circuit makes the addition of diode logic circuits very simple as shown in Figure 5. To obtain a 3-terminal *or*-circuit it is only necessary to connect the three terminals to the input through diodes pointing towards *X1*. The amplifier will then produce an output pulse whenever there is a signal on any of the three input leads. To obtain a 3-terminal *and*-circuit, it is necessary to add only two additional diodes connected to the emitter just as *X1* is. Each of the diodes is returned to -8 volts through a resistor corresponding to *R2*. Then the emitter can be raised above the peak point only when positive inputs are applied to all of the input leads and all three diodes are cut off. Inhibition can be obtained by means of an inverting transformer and another diode connected to the emitter and returned through the transformer secondary to a positive voltage. In the absence of any input the emitter is held below the peak point by diode *X1*. If diode *X1* were cut off the circuit would fire. However, if a positive pulse were fed to the primary of the inverting transformer, the added diode would clamp the emitter below the peak point and the transistor could not fire regardless of what happened to *X1*. These elementary logic functions are a complete set and all logic operations can be mechanized by a suitable combination of these elementary ones.

For memory purposes, a delay line is suggested with the transistor amplifier described above used to amplify and retime the delayed signals before they are recirculated. For the kind of memory that is ordinarily provided by a flip-flop the regenerative amplifier is suggested with its output fed back to its input through a simple delay network. This device has the property that when it stores a one it puts out a continuous train of digit pulses and when it stores a 0 puts out nothing. The reason that the transistor flip-flop itself is not recommended for storage is that when a transistor is left locked up in a high-current state it takes a great deal of power to unlock it and it is easier to obtain that power from a steady-state clock signal than an information containing signal that would have to be supplied by the computer. What amounts to permanent storage is obtained and yet the transistor is still turned off every microsecond by the master clock.

Proposed Building Blocks

In the first experimental work, only the amplifier was packaged and the external logic circuits and the delay lines were mounted external to the packages. This is why the multiplier took half of a relay rack to mount. To achieve miniaturization consistent with the size of the transistor itself, all the components must be packaged efficiently. Unless a wide variety of packages are developed one must be contented with a relatively small number of available functions and achieve all results with that restricted set. This minimizes the different types of packages required in the computer but probably results in using a greater number of tran-

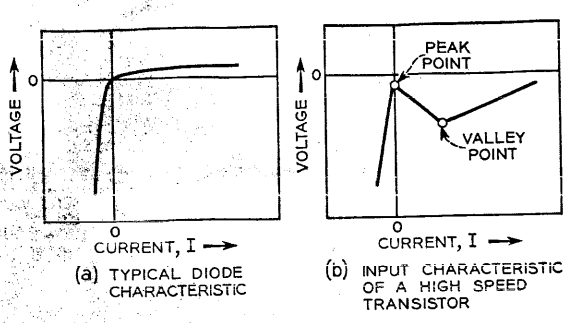
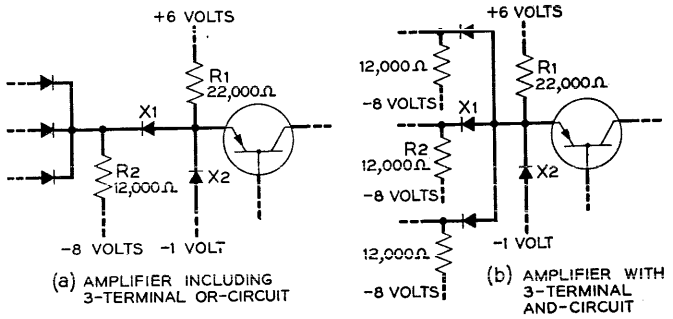


Figure 3 (left). Input characteristics



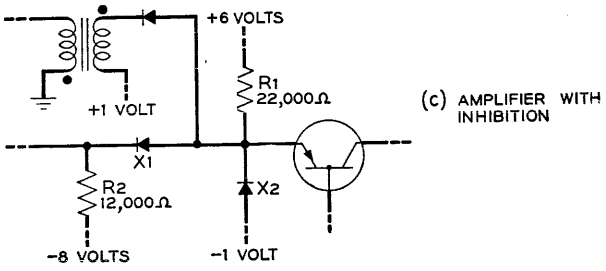


Figure 5 (right). Basic logic circuits added to amplifier

sistors than would be required if a wide variety of functions each designed for a minimum number of transistors were included in the available set.

The set of functions shown in Figure 6 is proposed as a reasonable set for the arithmetic organ of high speed computer. Each package is complete and can drive several packages in parallel. The first package is a 2-terminal *or*-circuit with pulse amplifier. The second is a 2-terminal *and*-circuit with pulse amplifier. The third package proposed is an inhibitor circuit which will regenerate the signal on the lower lead unless there is a signal on the top lead in which case there will be no output at all. In serial arithmetic units some memory is required and the fourth package is proposed as a replacement for the ordinary flip-flop. If a pulse is put on the one lead the bit cell develops a train of timed digit pulses until it is shut off by a pulse on the 0 lead. The fifth package is used to build up memory components for more than one bit. It consists of the transistor amplifier with a simple delay network to delay the output pulse by 1-digit time. If small delay lines were available this fifth package would not be necessary. But until very much smaller delay lines than are now available are developed, such a package will be very attractive in applications where space saving is important.

One of the reasons that so much emphasis is put upon the small size is that the transistors now available are temperature sensitive. It would complicate transistor design considerably if high-speed transistors had to be made at this time that would operate at very high temperatures. Fortunately, the transistor because of its low power operation does not itself generate much temperature rise, therefore, the transistor may not have to operate at temperatures above ordinary room temperatures. However, applications are foreseeable in which the effective room temperature may be considerably above that, for example, of a university laboratory. For these applications the fact that 400 or 500 transistors with associated circuits can be put in a volume of the order of a cubic foot and that the entire power dissipation of such a computer may be of the order of ten watts gives us the hope that an entire computer can be placed in a box small enough to be held at a reasonable temperature.

Insofar as predictions for the future are concerned an optimist might subscribe to these: the power per stage will be reduced to the order of 100 microwatts; repetition rates for pulses will increase to 10 megacycles and perhaps 50; miniaturization will be so complete that no application of a digital computer need be held up because space is not available; reliability will be so improved that systems with 100,000 transistors will be practical and the venturesome will contemplate systems containing 1,000,000 transistors.

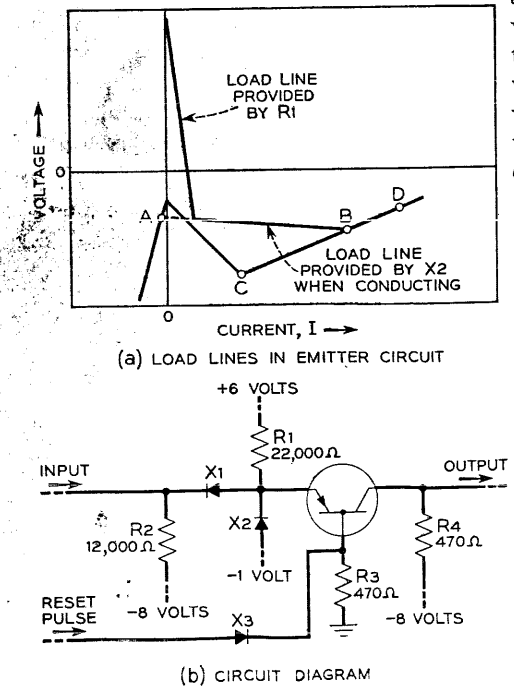


Figure 4 (left). Schematic of pulse amplifier

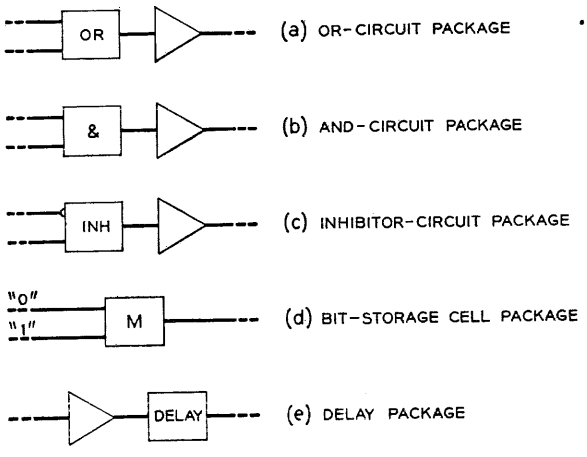


Figure 6 (right). A set of functions for a digital computer

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Discussion

I. L. Auerbach (Burroughs Adding Machine Company): Could you tell us the temperature at which you are encapsulating the transistors and crystals and the effect it has on their life?

J. Felker: I do not know what that temperature is. I know it is possible to put these in the capsule and still have a satisfactory yield. In other words, we have working units that have been put in plastic.

J. C. McPherson (IBM): On the circuits you have already built, what is roughly the ratio of diodes to transistors?

J. Felker: The basic amplifier requires three diodes to help the transistor operate as an amplifier. Then if you put the logic functions on also, you can get by with as few as three additional diodes per transistor. If you want to use more logic circuits, the number of diodes will go up. But I would estimate something like eight to ten diodes per transistor in a balanced machine design.

F. C. Mullaney (ERA): Your diagram showed certain values on the components. Must these values be changed as different transistors are inserted in the circuit?

J. Felker: No. In our multiplier, for example, which had 43 or 44 transistors in it, all the amplifier circuits were identical to the extent that we could get them so, and all the transistors were interchangeable to the extent that anyone tried to interchange them.

E. D. Lawler (Naval Air Development Center): From what I have read, there are a number of different types of transistors. Could you specify exactly the one you used in the circuit?

J. Felker: The transistor that was used in these circuits carries the number, M-1734; the short title is "the high-speed transistor." I might mention that it is a point contact transistor, not the junction-type transistor.

Digital Computers: Present and Future Trends

JAY W. FORRESTER

THE Program Committee asked me to summarize the present status of digital computers; also to point up the better features of the machines described at this Conference, and to forecast trends to be expected in the future.

We might start by determining where the digital computer field now stands along the road of progress. The first round of electronic digital computers has been completed, with a variety of machines showing varying degrees of success. The competitive spirit and rivalry between groups engaged in computer development has been strong in the past. We have met at this Conference for a frank discussion of the good and the weak points of the various machines. Some papers have stressed the good points and the successes. Others have stressed the future objectives. Still others have given us a picture of the shortcomings and weaknesses of the existing machines and frank, although conflicting, evaluations of what these results indicate for the future.

Present Status

A comparison of the present status of the digital computer field with any of our older branches of engineering shows that we are not far advanced. We are firmly on the threshold of a new field, but the digital computer work has reached no real maturity. Up to the present time people have made impressive contributions to the field of digital computation. Digital computation, however, has not yet made nearly the contribution to society that our enthusiasm might lead us to believe.

Maintaining the proper perspective here is important. It is entirely possible that the work of the world which has been accomplished by the modern automatic digital computer could have been more than accomplished if the man hours thus far put into the development of digital computers had instead been applied to the solution of the ultimate problems. We must look upon the results thus far as an investment in the future. We have first models of a new type of machine. There is no reason to believe that they are relatively any more advanced than were the first models of automobiles, the first aircraft, or the first radio sets.

Some rather remarkable attitudes have existed in the digital computer field. First models, without any tested predecessors, have been scheduled for production. Contracting officers have even bought first experimental machines on the assumption that they would be final production models rather than being useful primarily for evaluation. In few other fields would this be done. A first model of a new airplane is built for testing and evaluation, not for delivery to the fighting Air Forces or to an airline.

The machines reported at this Conference might properly be looked upon as exploratory models for evaluating physical techniques and design procedures, as vehicles for the assembly and training of organizations capable of designing computers, and, to the extent that the machines operate successfully, as devices for training people in the use of digital computers.

Big steps have been taken, but they represent only a beginning on the road ahead. We have first models of machines, but we don't even have adequate or recognized evaluation criteria for their assessment or discussion.

We are almost without experience in using these machines outside a development laboratory atmosphere. Most of the machines are still under the care of their designers or operated in a sympathetic research laboratory environment.

Until now we have been occupied by plans for proposed machines. In this new period ahead when the electronic digital computer is being evaluated, we will obtain results from the first round of computers and interpret these results for guiding future models of machines.

In building the first generation of electronic digital computers, we have learned the magnitude of the engineering involved. In the past 5 years, time estimates in the digital computer field have been a standing joke. Many of the cost

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estimates have been absurdly low. The importance of high quality engineering is pointed up by a few much publicized machines which have never reached successful operation and by the maintenance problems of those machines which have operated. There exists now a much better appreciation than we had a few years ago for the design stages, component testing, and engineering development that lie between the block diagram and the operating computer.

There are already signs, however, that we may not have learned enough by this experience. The underestimation of construction time is giving way to an underestimation of the time necessary to place a machine in successful service. This, in turn, is followed by underestimation of the time which will be needed for learning how to use the computer for productive output.

Digital computers have varied considerably in the amount of shake-down time required. Perhaps one of the better experiences is the ERA 1101. The Whirlwind I machine has required a year to reach its present reliability. Mark III was announced 2 years ago, and you have heard the report on its operation. On the other hand, the EDVAC and the BINAC are still undergoing adjustment and modification. SWAC was dedicated over a year ago and is still under test operation.

Difficulties have resulted largely from more emphasis given to performance characteristics than to certainty of operation. The number of storage registers, the speed, or any of the other performance characteristics are certainly secondary to the question of whether or not the machine will, in fact, function.

Organizations have often undertaken too ambitious a program for the facilities and engineering manpower available. There are only a few examples of modest and exploratory beginnings in the digital computer field. The Burroughs Adding Machine Company people have reported on their program of learning by assembly of their trial machine out of test equipment units. The SEAC machine, the EDSAC, and the Ferranti machines have set modest objectives which were discharged without becoming involved in unduly elaborate devices. The ERA 1101 and the International Business Machines Company Card-Programmed Electronic Calculator were done by commercial organizations basing their designs on somewhat similar equipment already developed.

Table I. Storage, Cost-Performance Criteria

Storage Type		$/Bit	$/Performance Unit
Magnetic drum	(1949)	0.15	1,200
Acoustic line	(1950)	1.75	500
Electrostatic	(1951)	8.00	160
? ?	(1956)	1.00	3

Evaluation Criteria

Various machines must now be evaluated. There are many machines to be compared, but for the most part we find ourselves without any test or comparison criteria. There is fair agreement regarding the definitions of speed and storage capacity in digital computers. The time has come for more sophisticated criteria of comparison. In the papers at this Conference, each group has used its own definition for reliability of its equipment. It would be almost impossible to make a comparison between the different machines based on the data. Likewise, there can be no significance in cost figures, unless accompanied by a measure of performance and reliability. We discuss the number of vacuum tubes in a machine, but this in itself lacks significance unless we have a measure of the utility of those tubes, in other words how much computation will they perform for us.

Storage Criteria

I might cite some examples of the kinds of criteria which will be useful. Consider first the storage systems. It has been customary to discuss storage systems in terms of capital cost per binary digit of storage capacity. This leaves out any concept of performance, and, since the access time is of first order importance, it might be better to use the criterion of cost per unit of performance. Table I illustrates typical numerical values. In the first column is cost in dollars per binary digit. This is capital cost and maintenance for a 5-year period and includes associated control equipment. For those applications which require large storage capacity without imposing demands for short access time, cost per digit is perhaps the proper and sufficient criterion. In dollars per binary digit, we find the magnetic drum most favorable, followed by the acoustic line and the electrostatic tube. A good measure of storage performance might be defined as:

$$\text{Performance units} = \frac{\text{Binary Digits}}{\text{Access time in microseconds}}$$

For high-speed internal memory, a more significant cost criterion would be dollars per unit of performance, and we then find the ordering of the three principal present-day storage systems reversed. Cost divided by digits of storage divided by access time gives us for the magnetic drum $1,200, for the acoustic line $500, and for electrostatic tubes $160. These are approximate values, but typical of present-day systems. Part of my assignment here is to predict trends, and I suggest that in the next few years, we should expect to see the cost per unit of performance reduced to as little as $3. This improvement may result from advancements in solid state physics which will yield both simplicity and higher speed.

Design Efficiency

Another criterion is needed for measuring the machine design effectiveness. Digital computers discussed at this Conference differ by a factor of only 2 or 3 in complexity but by orders of magnitude in speed. We find that the higher speed machines are more efficient in terms of the work they will perform per unit of equipment. We can draw here an effective parallel with the internal combustion engine. The man with a very small job to be done or who will use his computing machine only occasionally is rightly interested only in total complexity and cost. Let us compare this with a one horsepower outboard motor for a fishing boat. In the engine, horsepower represents work done in a unit of time and can be likened to the arithmetic operations per unit time or speed of a digital computer. In the outboard motor, we have a small, simple inexpensive machine which may weigh 20 pounds per horsepower and costs $40 per horsepower. In designing an automobile one certainly doesn't use a multiplicity of outboard motors. Instead of 20 pounds per horsepower, the automobile engine weighs about 5 pounds per horsepower. Instead of $40 cost per horsepower, the automobile engine may run $3 to $5 per horsepower.

We find a similar situation in the performance per unit equipment or in the cost per unit of performance in the digital computer. Table II shows the approximate order of magnitude for various classes of present-day computers in terms of the performance efficiency index which I define as the operations per second divided by some standard unit of equipment. Deciding on a unit of equipment is difficult and controversial. For present-

day machines the vacuum tube cathode might be taken as this unit, as long as the complexity and cost of the computer is related to the number of tubes. For the drum computer this index is about *0.03;* for the acoustic line computer about *0.5;* and for the parallel electrostatic tube computer about *1.2.* Again, if I should make a prediction for 5 years hence, I would say that we can reach an index figure of about 20 operations per second per unit of equipment. This index is meant to be comparable with the others, but it may be necessary to redefine the unit of equipment if the vacuum tube at that time has been replaced by other elements. This higher efficiency should be achieved with higher speeds and a substantial reduction in complexity. Table II also shows approximate capital cost per unit of computing speed for the various types of machines.

The index of efficiency can be used advantageously in determining the utility of auxiliary equipment for a machine. One is often tempted to make a special device for converting number bases or a piece of terminal equipment to simplify the work of the computer. Such equipment may operate at a very low duty factor and do a job of which the main machine is capable. One should ask himself how the average operations per second, averaged over a year's time, per unit of equipment in the special device, compares with the above index for the main machine. It will often be true that the simple job is more efficiently handled by the complex central machine.

Reliability Criteria

Considerable emphasis in the papers of this Conference has been placed on digital computer reliability. We do not even have a definition of reliability, to say nothing of criteria for measuring those factors which produce reliability. To some people reliability is measured by the percentage of time that the machine is not in the hands of maintenance men. To others reliability is measured by the frequency of random mistakes in the results. These are two very different concepts. In many ways the frequency of random errors is much more important than the percentage of inoperative time, and yet we have heard almost nothing about this during the last 3 days. In the papers, the percentage of inoperative time has been used as an indication of digital machine quality; it is just as much a direct measure of the expertness of maintenance which the machine receives. We need a measure for the maintenance effort put into a digital computer. I suggest that total number of men assigned to maintenance is not adequate, especially when we talk about machines which differ by four orders of magnitude in speed. It would seem more appropriate to measure the amount of maintenance the machine requires in terms of the man hours expended per million arithmetic operations usefully performed.

In some applications continuity of operation is of primary importance. Two definitions of continuity have been used: One definition measures continuity as a percentage of the total number of hours in a week. The other measures continuity as the percentage of scheduled operating time without penalty for scheduled maintenance time. Both definitions are useful if properly understood, but both have an important and fundamental fault in the impression they create. Continuity of performance should be measured in the percentage of inoperative time rather than in the percentage of operating time. If asked how good your watch is, you don't say that it gives 1,439 minutes correct out of the day, but rather that it loses 1 minute per day. Ratios of inoperative time are better indices of quality than ratios of operating time. I suggest that a 2 to 1 ratio in engineering quality exists between 30 per cent and 60 per cent inoperative time and also that a 2 to 1 ratio exists between 5 per cent and 10 per cent inoperative time.

Error Frequency

There has been little discussion of reliability in terms of frequency of errors. There seems a strong tendency to measure mistakes in terms of errors per unit of time. The digital computer profession stands in awe of the very enviable record of the Bell Telephone Laboratories relay computers. These are reported to have made only one or two errors not caught by their checking equipment in the period of 5 years. A better criterion than the errors per unit time might be the millions of operations carried out between errors. On this basis the Bell Telephone Laboratories record stands, according to legend, at something like 35 million operations per mistake. To equal this record, some of the modern machines need to run error-free for a period of only an hour and a half, and this, indeed, has been done.

I think that as a future trend we can expect great strides in the reduction of inoperative time and the elimination of isolated machine mistakes. It is an unusual person who can make 500 arithmetic computations on the desk calculator between errors. Machines built today can do millions of operations between errors, and the next 5 years may bring us machines with reliability against random mistakes in the decade above 1,000 million operations per error. This should be accomplished without unreasonable cost. I therefore agree with the comments on the EDSAC by Mr. Wilkes and those on Whirlwind I by Mr. Everett that checking devices will become unnecessary, and disagree with the conclusions in the paper on Mark III by Mr. Poorte that internal checking is mandatory. The engineer here has a challenge to build a reliability into his computing machine comparable to that existing in other modern machines. The airplane engine operates 1,000 hours between overhauls and many times that between failures. Why not similar performance from a computer?

Checking

The papers at this Conference disclose two different attitudes toward machine checking and isolated errors. One group attempts to provide checking equipment which will stop the machine when a mistake is detected. The other group places its reliance on the prevention of mistakes. The choice apparently depends on the error frequency which is expected and on the type of application for which the machine is designed.

For a very high error rate, say a few thousand operations between errors, and therefore performance which is only one or two orders of magnitude above manual computation, a detecting and self-correcting error system is required. The self-correcting feature might be obtained by self-correcting codes which, so far as I know, have not been used in computing machines. Computations on a self-correcting basis can be programmed and this has been done.

For a medium-error rate, which might be a million operations between mistakes, self-checking, either built in or programmed, is indicated. For short sequences such a machine has a good probability of getting a correct answer, and problems can be rerun and the answers compared if necessary.

For a small error rate, which might be one mistake in ten million or one hundred million operations, programmed checks where applicable are entirely adequate.

For a negligible error rate, which we might call one error per thousand million operations upward, it is unlikely that any

attention to checking is required.

The choice between detection of errors and the prevention of errors depends a great deal on the application of the machine. In ordinary scientific and business applications, the matter can rest entirely on studying the economics of how to assure a sufficiently reliable result. Built-in checking equipment may be desirable, but the complexity should be weighed against duplicate solutions of the problem. The equipment efficiency criterion which I referred to earlier is a helpful guide in making this decision. The choice must be substantially influenced by the desirability of having a logically simple machine which is easy to understand and maintain. One departs rapidly from the simple machine as checking methods are introduced.

Very different considerations apply to digital computers intended for real-time control applications. A machine intended for military or industrial control must have a high probability of continuously correct answers. This means either a self-correcting error system or a negligibly small error frequency. Error detection alone is unsuited where the answer is valueless unless obtained at the time of the attempted solution.

Of the machines reported at this Conference, only the Whirlwind I was designed specifically for real-time control and an error frequency low enough for that application. Of the scientific machines, it appears that the IBM Card-Programmed Electronic Calculator, the ERA 1101, the Ferranti machine, the EDSAC, and the SEAC are getting satisfactory operation without built-in checking equipment. As near as I can tell from the papers, the other machines depend on built-in checking, or are as yet untried in operation, or have presented serious reliability difficulties.

Electronic Reliability

Consider now some of the factors affecting electronic computer reliability. The unreliability of electronic equipment has reached almost crisis proportions in military equipment of all kinds. Because of the special need for reliable performance in the digital computer, the digital computer engineers may be forced to evolve methods of insuring reliability which can help to alleviate the poor performance in other branches of electronics.

We do much talking about the unreliability of tubes and components. It seems to me, however, that the greatest obstacle to good electronic equipment is the frame of mind and attitudes of those participating in its design and procurement. No one will admit to being disinterested in reliability, but the fact is that theoretical performance, availability date, cost, and size are almost always placed ahead of reliability. The customer and the development engineer share the blame. It is so much easier to put definite numbers on storage capacity, speed, delivery dates, and cost, and these can effectively be used in publicity and the procurement of contracts and the appropriation of funds.

For lack of suitable criteria, reliability has not even been defined, much less evaluated. It is a controversial subject, resting on professional opinion rather than measurement. Reliability cannot be tested in a few hours or days as can other performance factors. The important aspects of reliability, such as freedom from errors and ease of maintenance, need to be evaluated under the conditions of the ultimate application rather than in the manufacturer's plant. Poor reliability is often dismissed on the basis of inadequate maintenance, unavailability of proper test equipment, and a multitude of other factors which either should have been foreseen as likely by the manufacturer or remedied by the customer.

Another difficulty here is that no one ever seems to be responsible for unreliable operation. It is charged to unavoidable and uncontrollable circumstances and accepted as inevitable. This again is an evidence of disinterest and defeatism. Once the proper attitude toward reliability has been developed in the supplier and the purchaser, we need have no fear for the reliability of the components. Funds and man hours would then be transferred from production of final equipment to the necessary development of suitable components. Adequate emphasis would be placed on good design and past failures would not be buried but studied for their weaknesses. I would caution against feeling that any magic will suddenly solve the dilemma of electronic unreliability. It will be solved only by hard work and long, meticulous, and expensive attention to detail.

We have had only a few suggestions at this Conference for specific technical ways for improving machine reliability. One of these is the marginal checking technique for depressing the performance margins of components to see if they do, in fact, have a safety margin between the normal operating point and the point of failure. We have had a favorable account of marginal checking in the Whirlwind I computer by Mr. Everett and Mr. Taylor. A modified form has been successfully used in the ERA 1101 where marginal checking is done by varying filament voltage. Varying filament voltage can be expected to catch deterioration of tube cathodes which accounts for half or more of electronic failures. Filament variation is much less effective than varying other voltages and pulse repetition rates for finding changed characteristics in resistors, crystal diodes, and other circuit elements. Mr. Poorte in his discussion of Mark III suggests that marginal checking would have been a help to them. I believe that a good marginal checking procedure will be absolutely essential in achieving a negligible occurrence rate of isolated errors. Marginal checking is a relentless tool in pointing out design weaknesses in a new machine. It gives good assurance of freedom from random errors occurring from components operating near their failure threshold. It is of almost no value in finding true intermittents, such as opens and shorts which depend on mechanical vibration. These mechanical intermittents are the most serious remaining obstacle to eliminating isolated mistakes in the digital computer.

Future Trends

We have heard the transistor proposed for the elimination of failures now attributed to vacuum tubes. The transistor does indeed look promising. I would caution against considering it a panacea. Vacuum tubes in some computer applications have a failure record as low as any thus far proven for transistors. The transistor will improve with time but, on the other hand, in a factory will not be made with the loving care given to the first laboratory models. As Mr. Felker has told us, the transistor may require rather special conditions in circuits which enhance its reliability. The same care and concessions to the shortcomings of vacuum tubes can do wonders for their reliability. With the proper use of marginal checking, the vacuum tube presents no serious problems except from open welds and short circuits. Again, with the proper attitude toward reliable electronics, these difficulties could be greatly reduced. Any of you who have seen the frantic haste with which vacuum tubes are assembled in the modern tube plant must wonder that they come anywhere near their present freedom from mechanical flaws. For computer use, the transistor is not so interesting for its small size and power consumption as for the unproven possibility that it can be

more free of intermittent changes in performance than the vacuum tube.

I now wish to mention several interesting items from the papers presented at this Conference.

Only one of the machines described, the IBM Card-Programmed Electronic Calculator, has had production and field experience. The International Business Machines people would have done us a great favor to have given us more information and numerical data on their service, maintenance, and field experiences. An important change is occurring in the ideas of how to administer a computing center and a computing machine. In the past, computer time has been so scarce and the changing from one problem to another so difficult, that only large blocks of time could be assigned to a user. In many computing centers, unless the client wants the machine for a month, he has almost no chance of getting machine time. With the new types of machines which can be changed in seconds from one problem to another, it is no longer necessary to put minimum limits on sizes of problems. The machine user can get time on the machine several times a week with intervening periods for studying results. This reduces greatly the amount of computation which must be done since he is under no compulsion to do large amounts of computing of uncertain future value for fear he will not have another opportunity. There is no economic foundation to the common assumption that the large computer is useful only for the large problem. The modern digital computer provides computation at a lower cost per unit of output than can be obtained by any other method. The lower economic limit for problem size is well down in the range of problems that are handled by manual computation.

Electrostatic storage tubes present a number of interesting aspects. Of the several electrostatic tubes receiving past publicity only the Williams' tube and the MIT tube seem to be in digital computer operation. If I may venture some comments on the Williams' tube situation, I think it points up a number of interesting facts in our attitude toward reliability and performance. The tube was developed by Williams' for use in a serial type machine which has successfully become the present Ferranti model.

Table II. Digital Computer, Cost-Performance Criteria

Computer Type		Efficiency: Operations/Sec. / Units of Equip.	Cost/Unit Performance: $ / Operations/Sec.
Drum	(1949)	0.03	3000
Acoustic	(1950)	0.5	750
Electrostatic	(1951)	1.2	250
? ?	(1956)	20	25

A serial machine of that type presents a favorable regeneration ratio and the tube can apparently be made to work well with proper care in engineering its circuits and environment. Even so, a special design of tube has been used. We see quite a different picture where the Williams' principle is being employed in high-speed parallel type machines. Here many groups are planning to use the Williams' tube, while few have adequate research facilities to fully explore the possibilities and limitations of the device in the more unfavorable parallel operation. With too small a research staff, each group is forced to a rather superficial attempt to place the tubes into a machine with the optimistic hope that operation will be satisfactory. Three years ago I saw the first read-around ratio test made on the first Williams' tube operated in this country, and the regeneration ratio was determined to lie somewhere between 32 and 128 cycles. We are at about the same place today.

If I might refer to my earlier comments on reliability and to the early motivation for using the Williams' tube, it seems that we have departed from two sound objectives. The Williams' tube was adopted as a quick and inexpensive way of obtaining storage with a standard electronic component. There is every indication that used with a small enough storage density and a high enough regeneration ratio it would in fact function well. In the meantime, however, the goals have been raised to the point where the tube may not qualify. Might it not be better first to accept what can be accomplished easily before battling for an elusive optimum?

For future trends it seems that the electrostatic tube, regardless of type, is but a transient on the stage and that it is scheduled to be replaced in the next few years by new developments in solid state physics. A strong contender is the 3-dimensional magnetic core storage array with a good possibility for ferroelectric storage.

In the future development of computing machines, we should expect more attention given to terminal equipment. Such a plea was made by Poorte in his paper on the Mark III machine. Present terminal equipment is relatively inadequate. Also our ideas about the use of terminal equipment and the kinds of results to be obtained from high-speed computers may be outmoded. There is still a tendency to want entirely too much tabulated data where we have rather unsatisfactory printing machines. As a way of avoiding part of this problem, I think the cathode ray tube output for graphical plotting should receive more attention. Also we should direct the machine to go further in data analysis to condense results into a small volume of information for human consumption.

For future trends in machine performance, it seems to me that there is no immediate hope for higher-speed video circuits. There can, however, be higher speed machines. A great deal of machine time can be saved by analyzing computing programs and providing special machine logic or facilities for saving time in the more frequent types of operations. In particular this applies to time-saving in the red tape operations where the *B*-box technique of the Manchester machine might be cited as an example of substantial progress.

Machine speed has increased by several orders of magnitude over the last 10 years. In the future we can perhaps get another decade in speed, but I doubt that more can be accomplished without a fundamentally new type of computer. The great steps in the near future, I think, will be in the direction of simplification without losing performance. It seems clear that the complexity of computers can and must be reduced.

Discussion

The following extension of remarks made from the floor was submitted in writing:

John W. Carr III (MIT): During the course of the convention sessions, informal sessions were held by representatives of some of the various computers now in operation and under construction, to discuss problems arising in programming. Present during part or all of these sessions were the following people:

M. V. Wilkes—University of Cambridge, England
J. M. Bennett—Ferranti, Ltd., formerly of Cambridge
D. J. Wheeler—University of Illinois, formerly of Cambridge

A. H. Taub—University of Illinois
H. E. Goheen—Moore School of Electrical Engineering, University of Pennsylvania
M. Rubinoff—Moore School of Electrical Engineering, University of Pennsylvania
V. G. Smith—University of Toronto
H. Gellmann—University of Toronto
R. A. Niemann—Dahlgren Naval Proving Ground
E. F. Moore—Bell Telephone Laboratories
J. Alexander—Argonne National Laboratory
W. F. Gunning—Rand Corporation
K. Uncapher—Rand Corporation
J. J. Connolly—Rand Corporation
F. M. Verzuh—Center of Analysis, MIT
C. W. Adams—Digital Computer Laboratory, MIT
John W. Carr, III—Digital Computer Laboratory, MIT
J. T. Gilmore, Jr.—Digital Computer Laboratory, MIT

Operating Procedures

The first topic to be discussed showed that there was a division of method in operating the various computers. Dr. Wilkes of EDSAC outlined the method used in his Cambridge laboratory by which the programmer normally prepares the punched tape but except on night shifts, leaves the performance of the program to a computer operator. C. W. Adams explained that his MIT group separated the programming, tape preparation and computer operation, leaving each to a specialist. On the other hand R. A Niemann stated that on the MARK III calculator it is customary for a programmer, aided by operators, to follow the program until it is correctly stored in the machine. Also, because of the length of problems under solution on MARK III, and the relative slowness of input, it does not appear either useful or efficient to use methods similar to those of Dr. Wilkes. The Illinois group has not operated long enough to have any set pattern of operation, but Dr. Wheeler, formerly of EDSAC, naturally showed sympathy with Dr. Wilkes' methods. However, Professor Taub of Illinois stressed the importance of the machine's working for the user, rather than vice versa, and suggested that carrying the Wilkes-Adams philosophy to the extreme might make the programmer the slave rather than the master of the machine. Dr. Wilkes and Mr. Adams agreed with the premise but disagreed with the conclusion. K. Uncapher of Rand Corporation stated that the present Rand philosophy in using IBM CPC machines was one similar to Dr. Wilkes'. No conclusion was reached, but it became apparent that this topic may well be a heated subject of controversy at future meetings.

Preventing and Locating Mistakes in Programs

The discussion on methods of minimizing mistakes in programming and in locating the mistakes which do occur opened with a description of the methods of error or blunder diagnosis used on EDSAC, as described in a book published recently by Wilkes, Wheeler, and Gill entitled "The Preparation of Programs for an Electronic Digital Computer, with Special Applications to EDSAC" (Addison-Wesley Press), and similar methods on the Manchester Computer (explained by J. M. Bennett of Ferranti Ltd.). Dr. Wheeler mentioned a new order-by-order print-out technique developed by Dr. Clippinger of Aberdeen, which traced the path of control through the machine, printing, however, only on the first passage of each loop. Mr. Adams proposed a post-mortem routine which consisted of printing out the contents only of those registers which had been changed during the running of the program.

Dr. Smith of Toronto compared a programmer with a blunder in his program with a lecturer at the blackboard who has become entangled in his analysis; and suggested that in both cases it might be better if both retired gracefully and returned after restudying the problem in the less strained atmosphere of his office.

Several suggestions were made as to methods of pretesting programs before they were run. The importance of double checking by a second programmer was stressed by Dr. Wilkes. Use of coding checkers with jobs similar to copy readers on newspapers was proposed by Dr. Smith. Dr. Carr proposed special checking programs to check only the logical structure of a program (where more blunders are likely to occur) with further arithmetic investigations being made later if necessary. Dr. Wheeler suggested that a programmer can more effectively check his own work if he puts the program aside for a week before checking it.

Of the special routines discussed, Cambridge's input program, the more elaborate conversion program of MIT's Whirlwind, the Manchester duotricenary (32-base) input, and the ORDVAC sexadecimal input were compared. Dr. Wheeler predicted possible changes in the ORDVAC scheme.

Dr. Wilkes proposed a "free address" system of coding in which only those words which are actually referred to by instructions in the program would be numbered, with all words being assigned to registers in sequence by the machine, and with the addresses assigned to the numbered words being inserted automatically where needed. This method would allow for corrections in programs without need for renumbering, and would generally free the programmer from his bondage to the machine numbering system. Various methods of representing subroutines by artificial instructions were also discussed, the assumption being that the input conversion routine would automatically select and assign addresses to the proper subroutines.

Universal Instruction Codes

The discussion on "Universal Codes" to facilitate communication between groups degenerated into a free-for-all over just how universal such a code should be. Dr. Rubinoff of Moore School defended a near-algebraic code, while others felt that codes applicable only to machines of one classification (such as single-address or three-address) might be more useful. It was finally agreed that actually two types of "Universal Codes" might be useful:

1. A truly universal code, perhaps similar to the Burks-Von Neumann device, that would explain the workings of a program independent of the type of address.
2. A generalized single-address code that would explain the workings of a problem in a language understandable to all users of single-address machines, with similar generalized 3- and 4-address codes.

Mr. Adams suggested the possibility of adopting a "universal" code which could be correctly interpreted not only by programmers but also by various different computers by means of interpretive subroutines. Such a scheme could permit the same program to be used on different computers, albeit at a loss of efficiency, and might aid in the adoption of a truly universal code for future computers.

Throughout this set of discussions, the absence of mathematicians and programmers from NBS, Eckert-Mauchly, IBM, Aberdeen, ERA, et cetera, obviously caused discussion to move in some particular directions rather than others, and therefore a complete sampling of programming opinion was not available. The consensus of the group was that further discussions of this type would be very helpful, and that formal sessions should be included in coming conventions, since the problems of programming at this point appear as yet mostly unsolved.